Estimation of Instantaneous Frequency Fluctuation in a Fast DVFS Environment Using an Empirical BTI Stress-Relaxation Model

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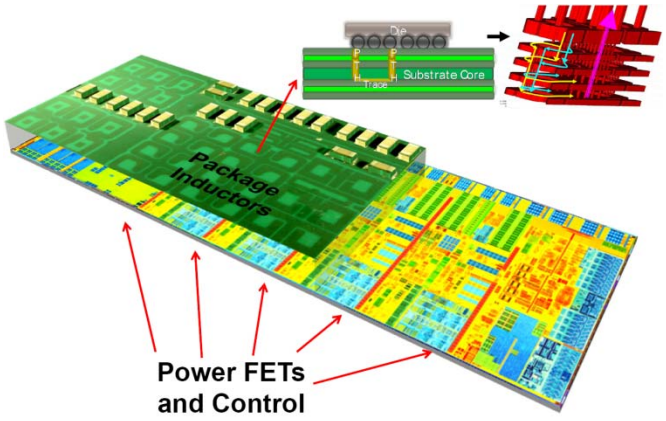
Purpose

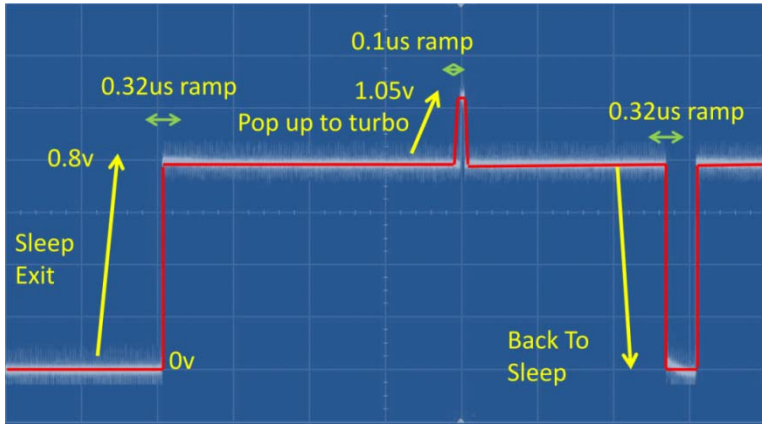
- **Understand how BTI aging impacts frequency guardband in Dynamic Voltage Frequency Scaling (DVFS) systems**
- **Develop an efficient model for estimating BTI-induced frequency degradation under fast DVFS transients**

Outline

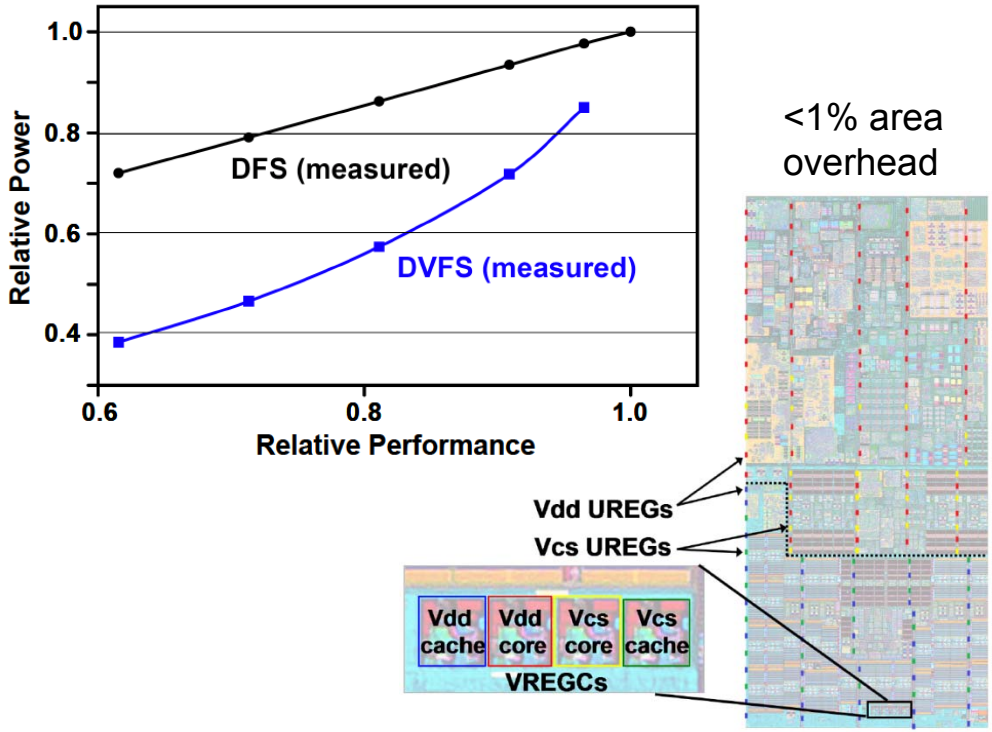
- Introduction to DVFS
- BTI Aging in DVFS Systems
- Proposed BTI Stress-Recovery Model
- Estimation of Frequency Fluctuation in a Real DVFS System
- Summary

DVFS Systems in ISSCC 2014





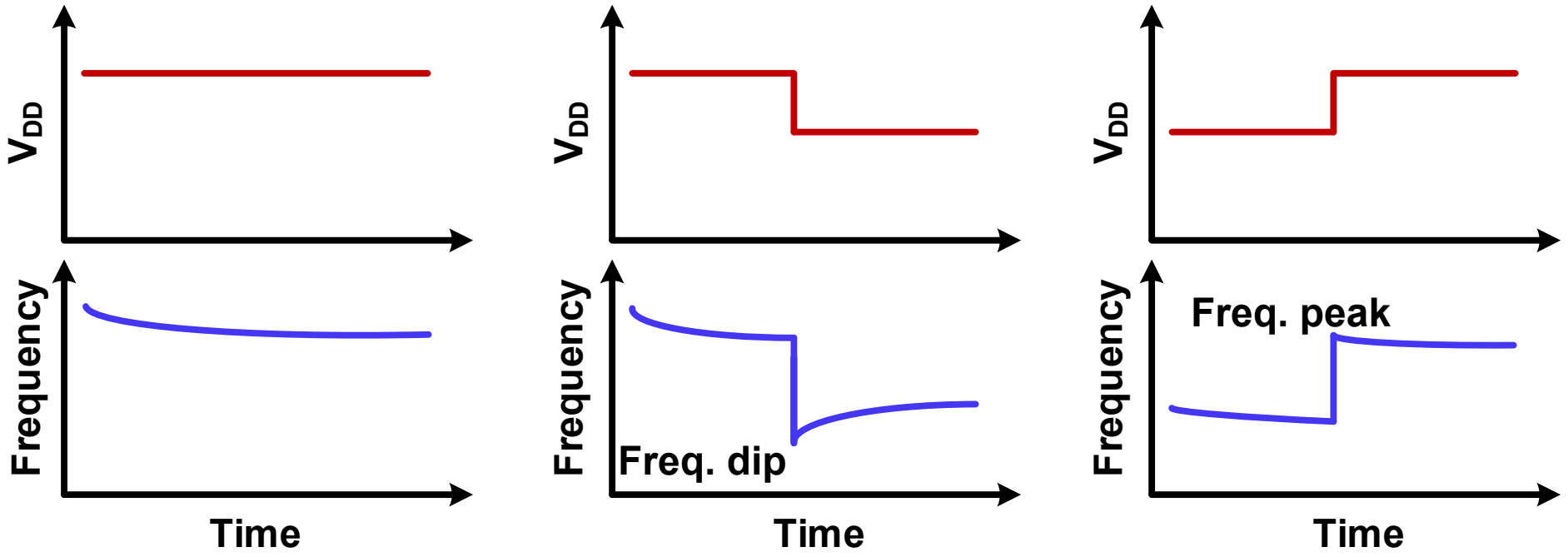
22nm Intel Haswell processor
N. Kurd, *et al.*, ISSCC, 2014



22nm IBM POWER8 processor
Z. Toprak-Deniz, *et al.*, ISSCC, 2014

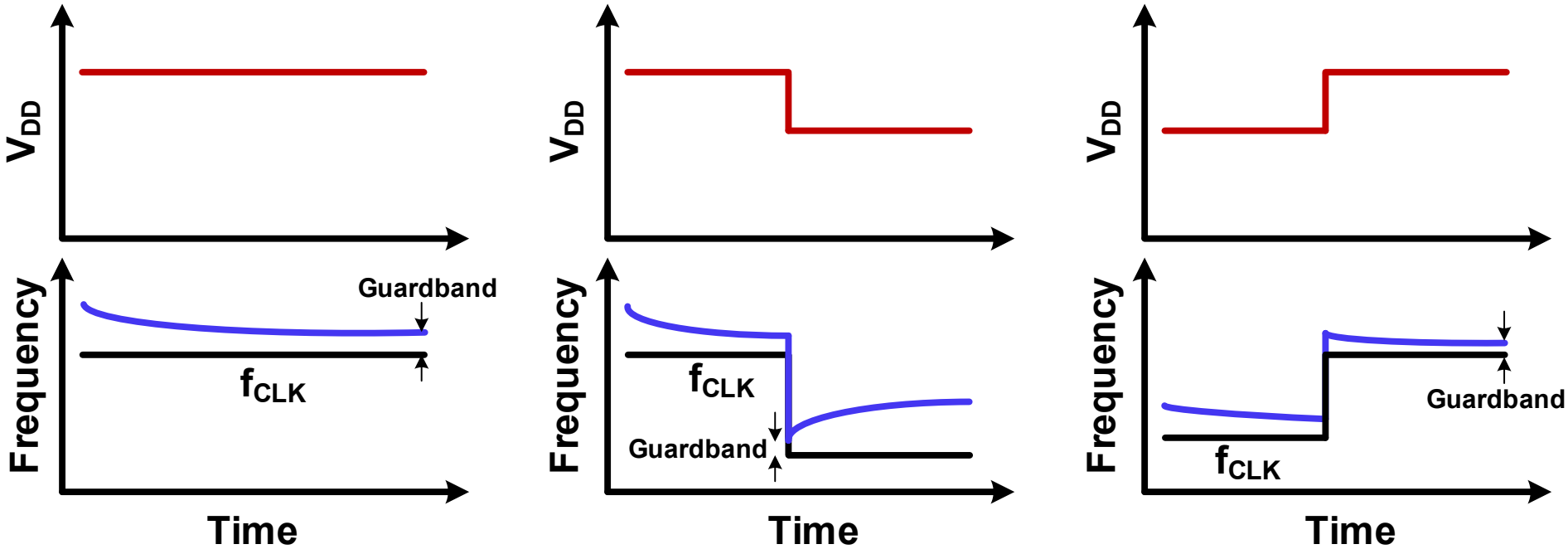
- Latest trends: On-chip distributed VRM (fast transients, supply noise suppression), per-core DVS, NTV/Turbo

Frequency Fluctuation in DVFS



- Constant V_{DD}: Frequency degrades with stress
- High V_{DD} to low V_{DD}: Freq. dips due to lower V_{DD} followed by recovery
- Low V_{DD} to high V_{DD}: Freq. jumps and then degrades

Frequency Fluctuation in DVFS



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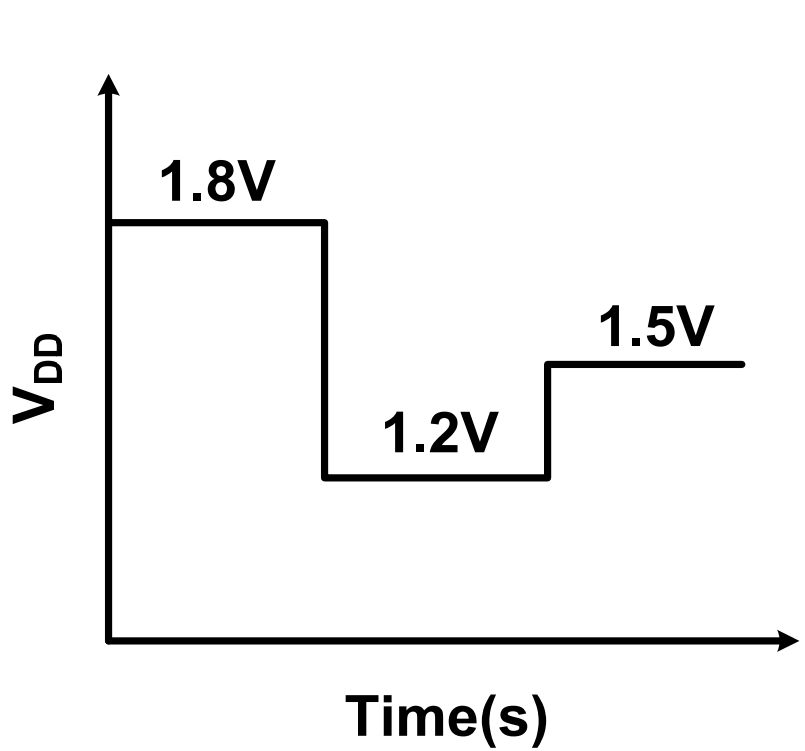
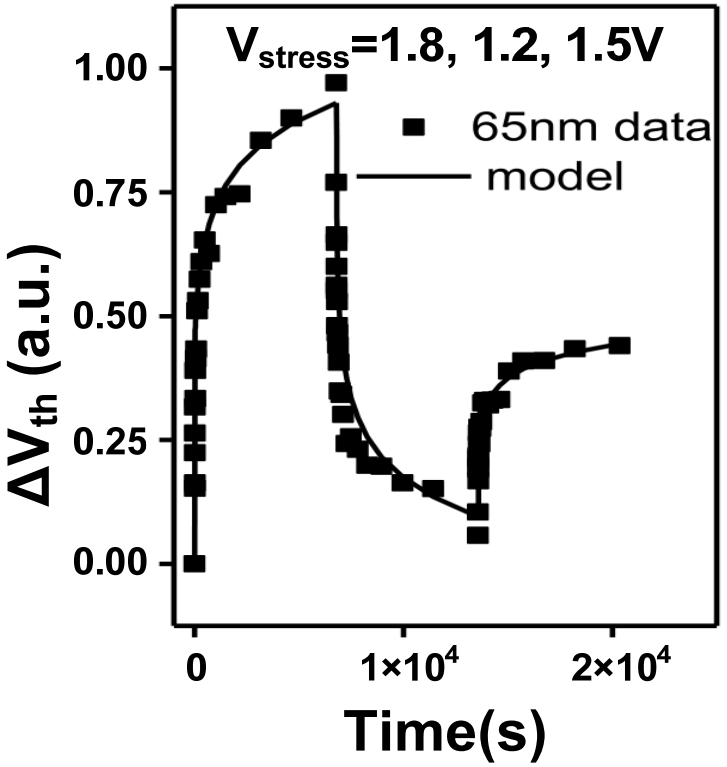
Previous Work on BTI Modeling under DFVS

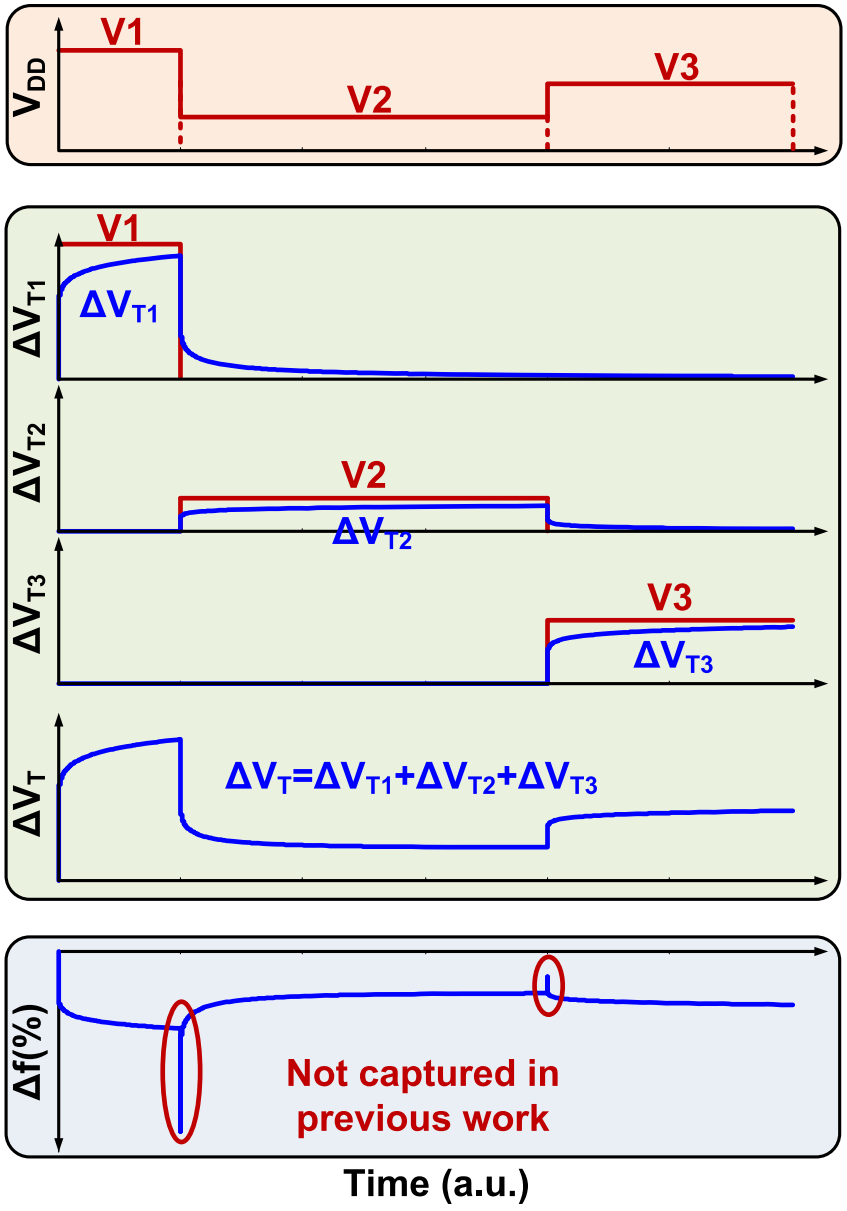




J. Velamala, *et al.*, TED, 2013

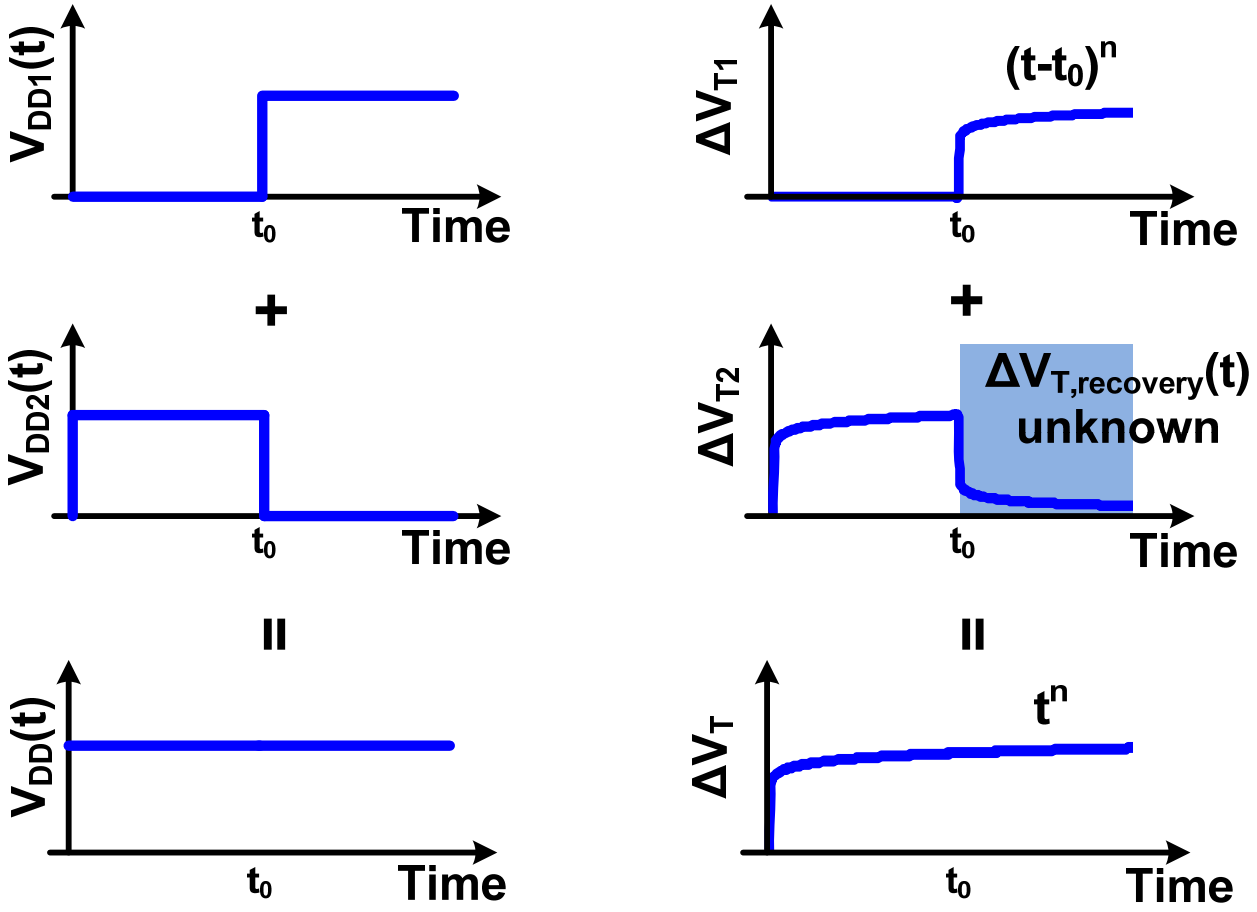
- **Limitations of prior work:**
  - **Focus was on long term aging**
  - **Frequency fluctuation in μs timescale was not considered**

Modeling Approach using Superposition



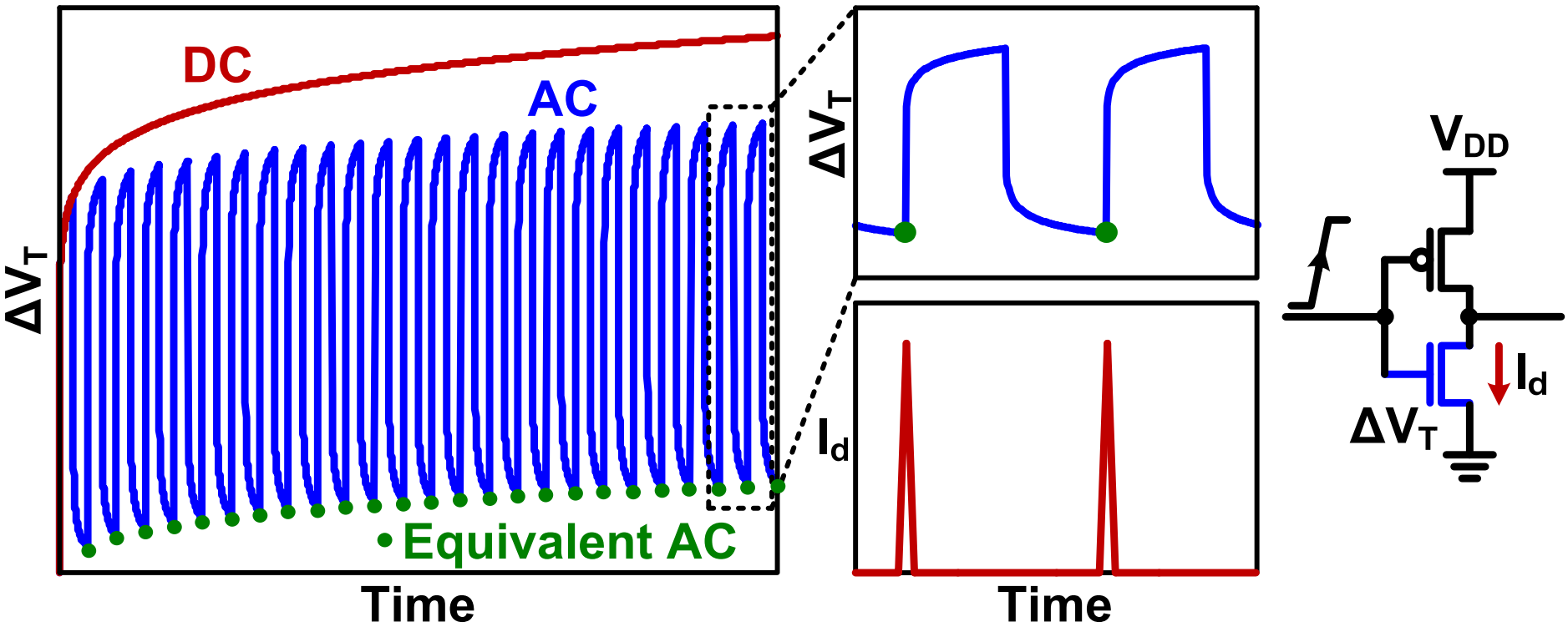
- Rationale for empirical superposition method :
  - Complicated V_{DD} trace can be broken down into multiple pulses
  - Suitable for both long- and short-term, DC and AC
  - Computation is more efficient, short runtime

BTI Recovery Model



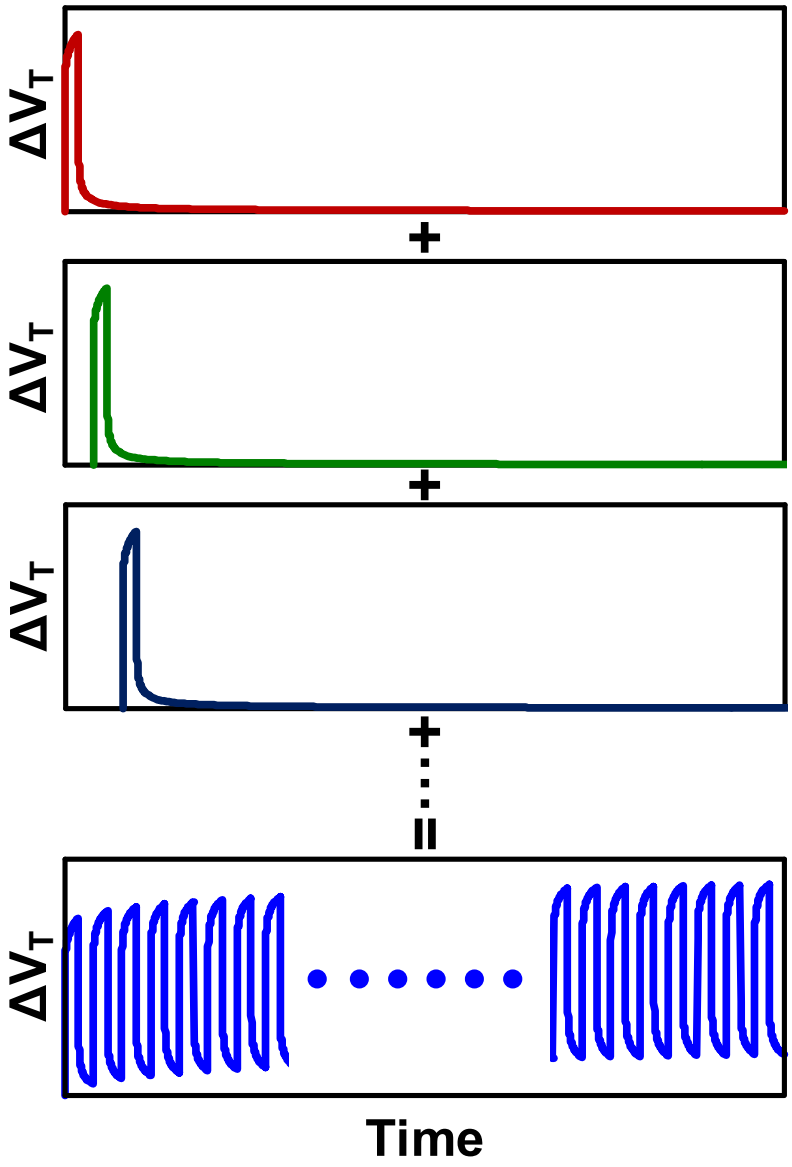
- **Stress model: t^n (power law)**
- **Recovery model derived from superposition property: $\Delta V_{T,recovery}(t) = t^n-(t-t_0)^n$**

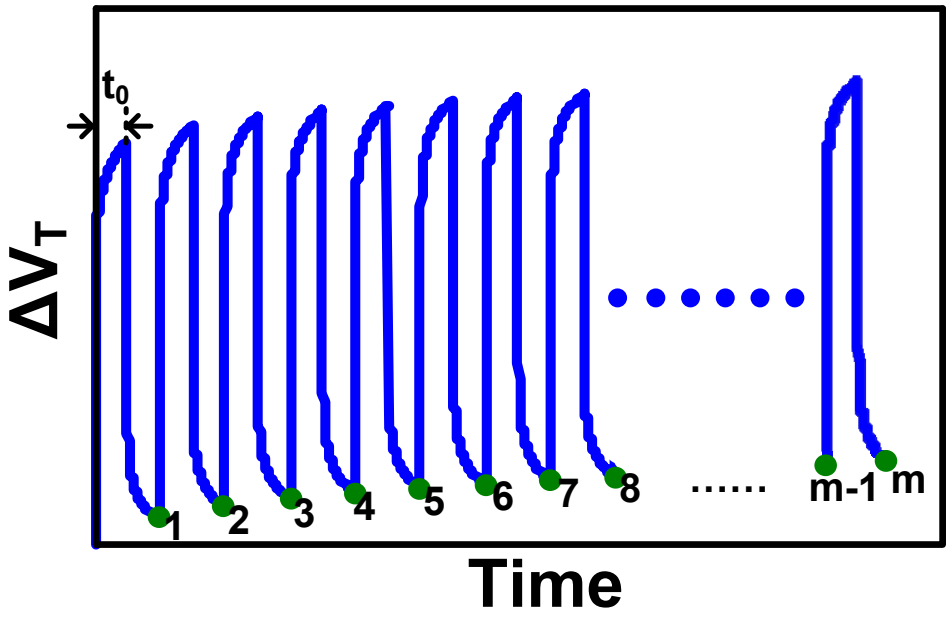
Incorporating Cycle-to-Cycle AC Stress



- Key observation: Transistor is in recovery mode just prior to switching
- Estimate lower envelope of the AC stress wave (only applicable to cycle-to-cycle AC stress)

Equivalent AC Stress Model

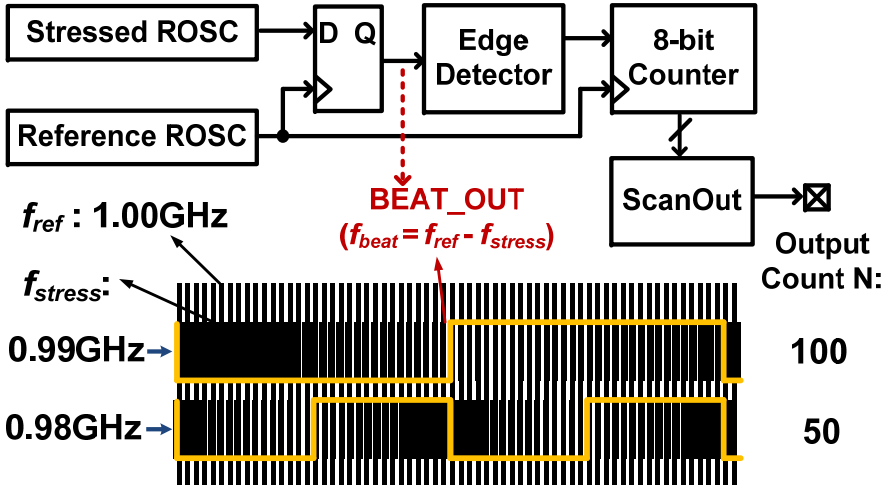


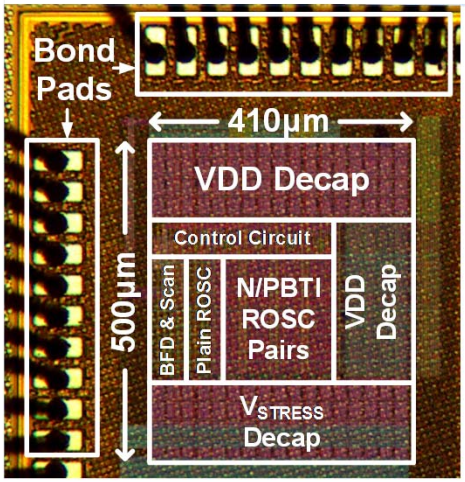


AC Stress Model
ΔV_T (at the end of m-th stress-relax cycle) = $A \sum_{i=1,2,...2m-1,2m} (-1)^i (i \cdot t_{s0})^n$

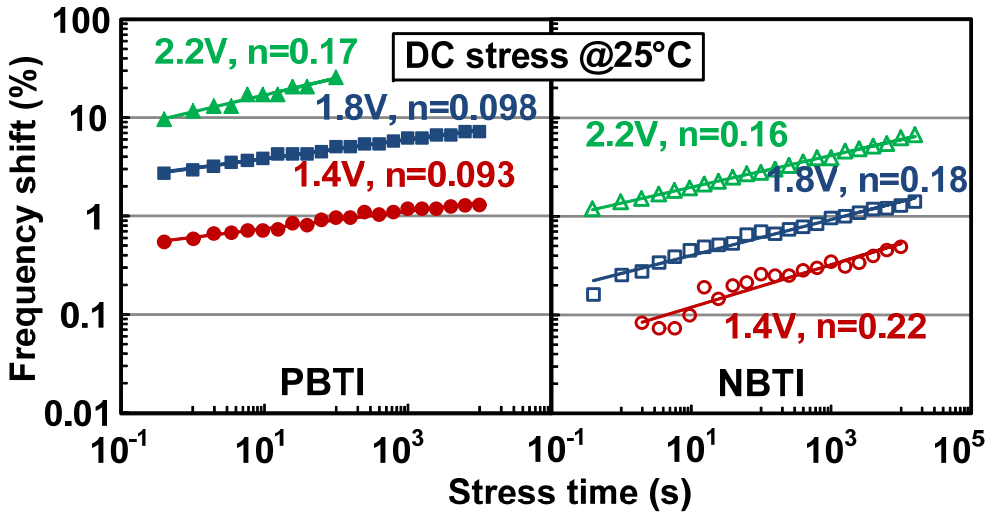
- Computation time < 1 min in Matlab

Extracting BTI Parameters from a 32nm HKMG Odometer Test Chip





Process	HKMG CMOS
Core / IO Supplies	0.9V / 1.8V
Stress Voltage	0.9V, 1.4V, 1.8V, 2.2V
Measuremt Voltage	0.9V
Area	500x410µm^2
Δf Resolution	>0.01%
Measuremt Time	>400ns
DUT Type	Core Devices



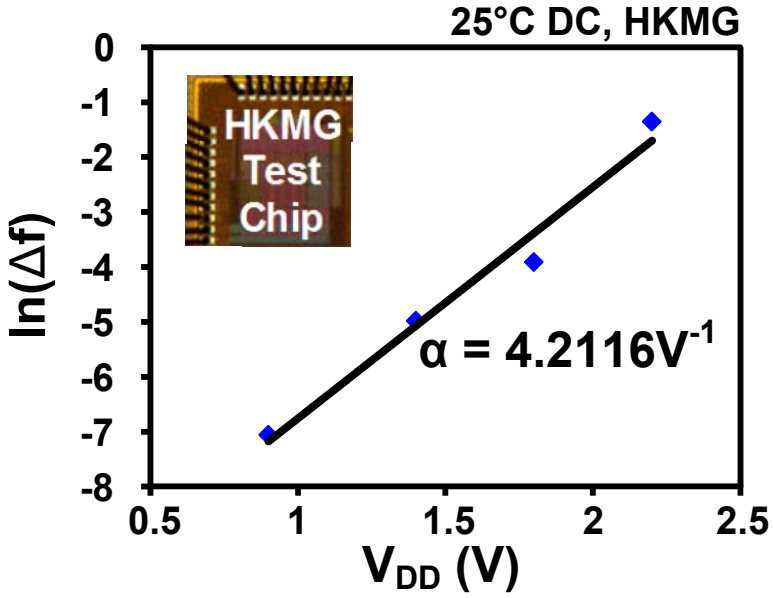
- **Frequency shift measured using beat frequency method**

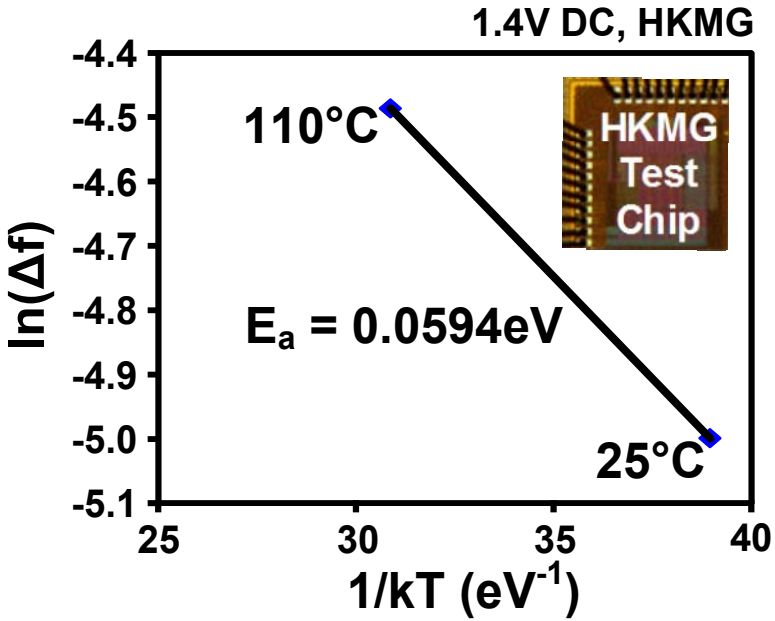
Voltage and Temperature Accel. Factors

ΔV_T vs. V_{DD}
$\Delta V_T(t) \propto e^{\alpha V_{DD}} \cdot t^n$
ΔV_T vs. T
$\Delta V_T(t) \propto e^{-\frac{E_a}{kT}} \cdot t^n$

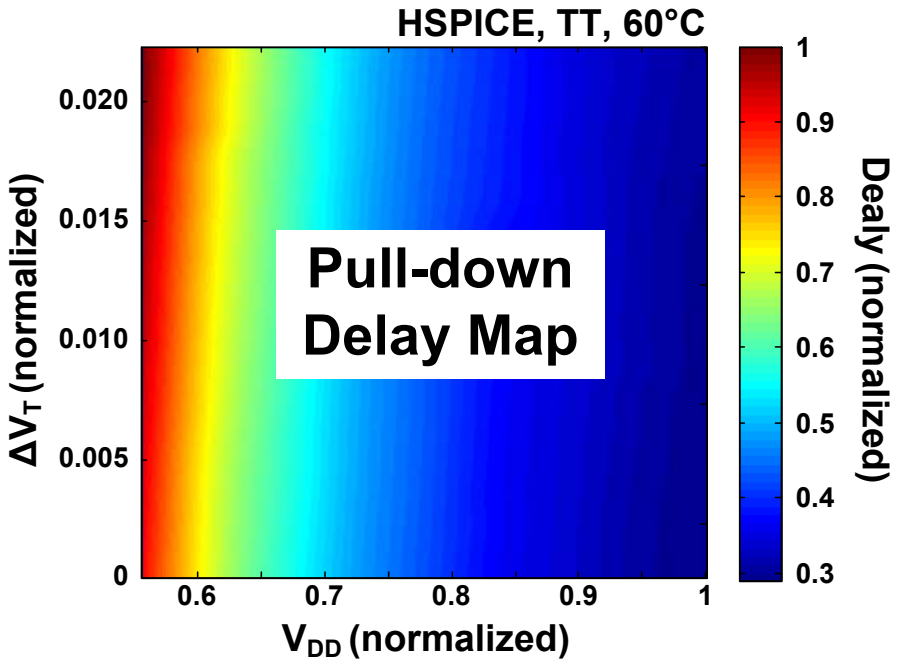
$$\frac{\Delta f}{f} = \frac{\Delta V_T}{V_{DD} - V_T}$$

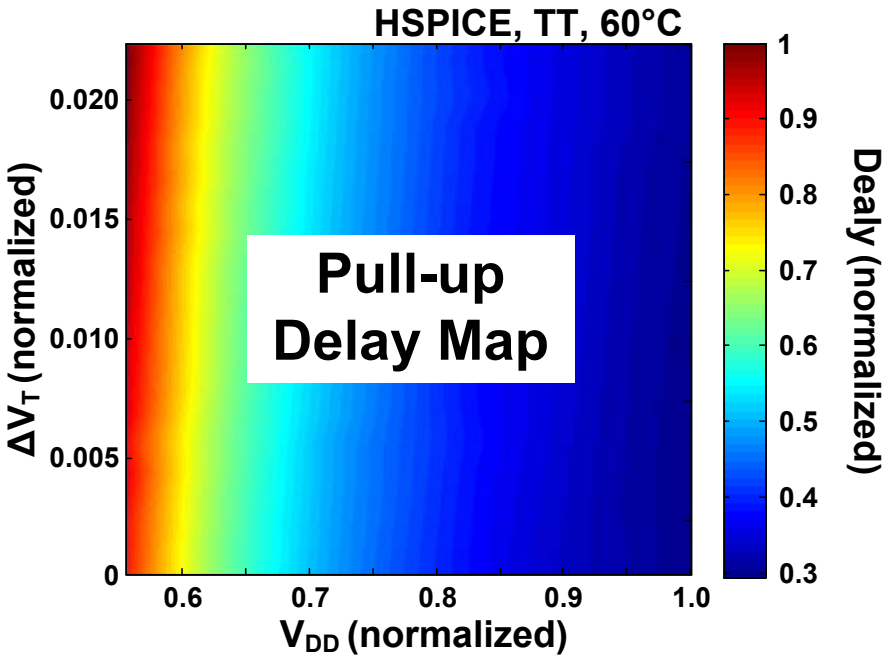
- **Calculate voltage acceleration factor and thermal activation energy from measured data**



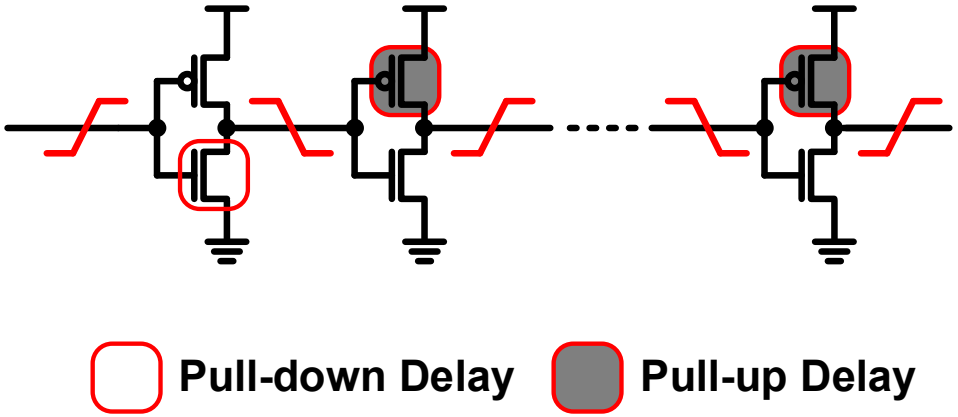


Translating V_T Shift to Delay Shift

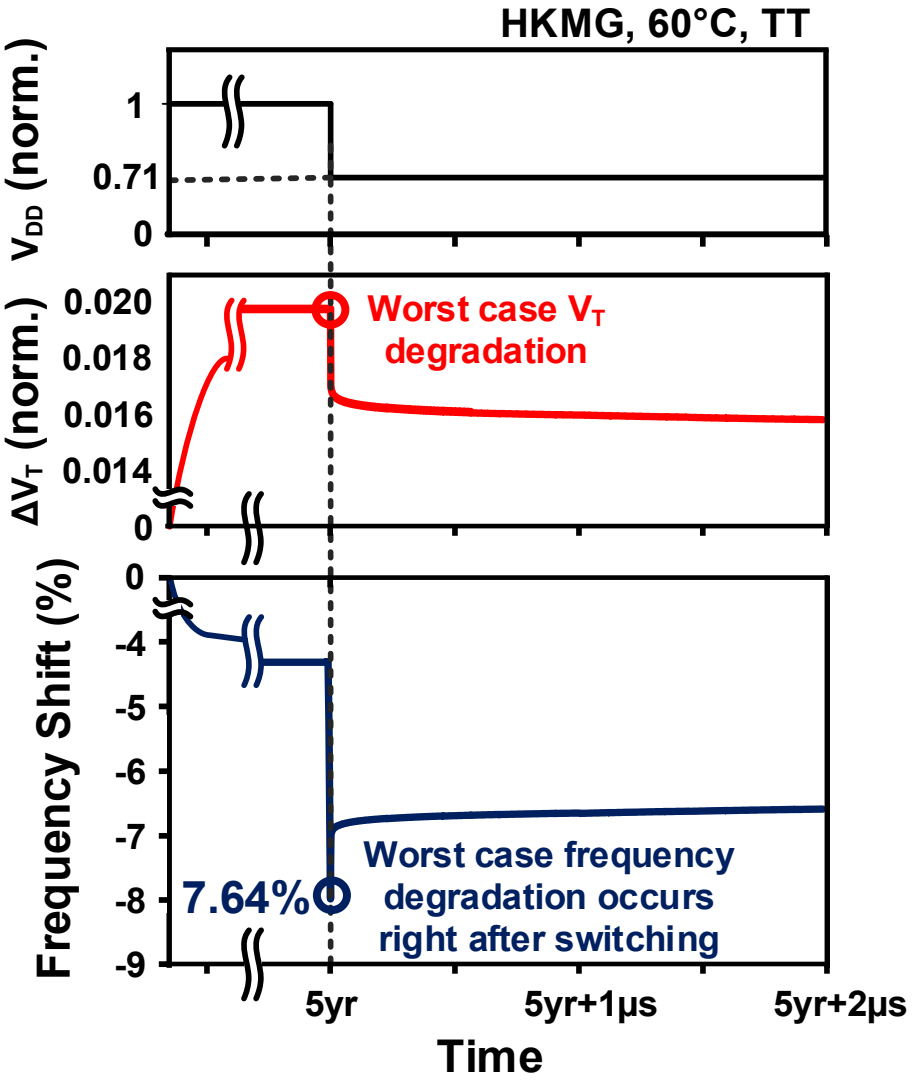




- ROSC mimics logic path
- Translate ΔV_T to pull-up, pull-down delay

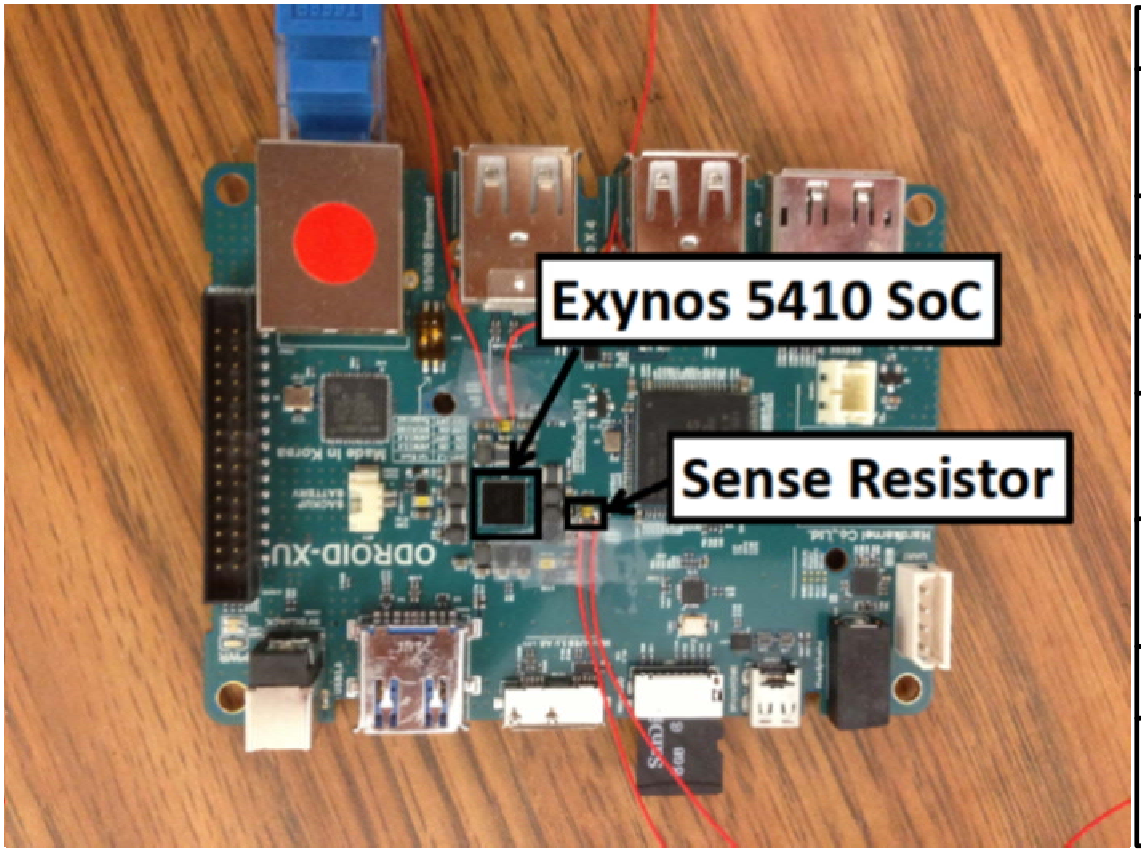


Worst-case Scenario Example



- Five years full V_{DD} DC stress → low V_{DD} active mode
- 7.64% frequency dip immediately after switch

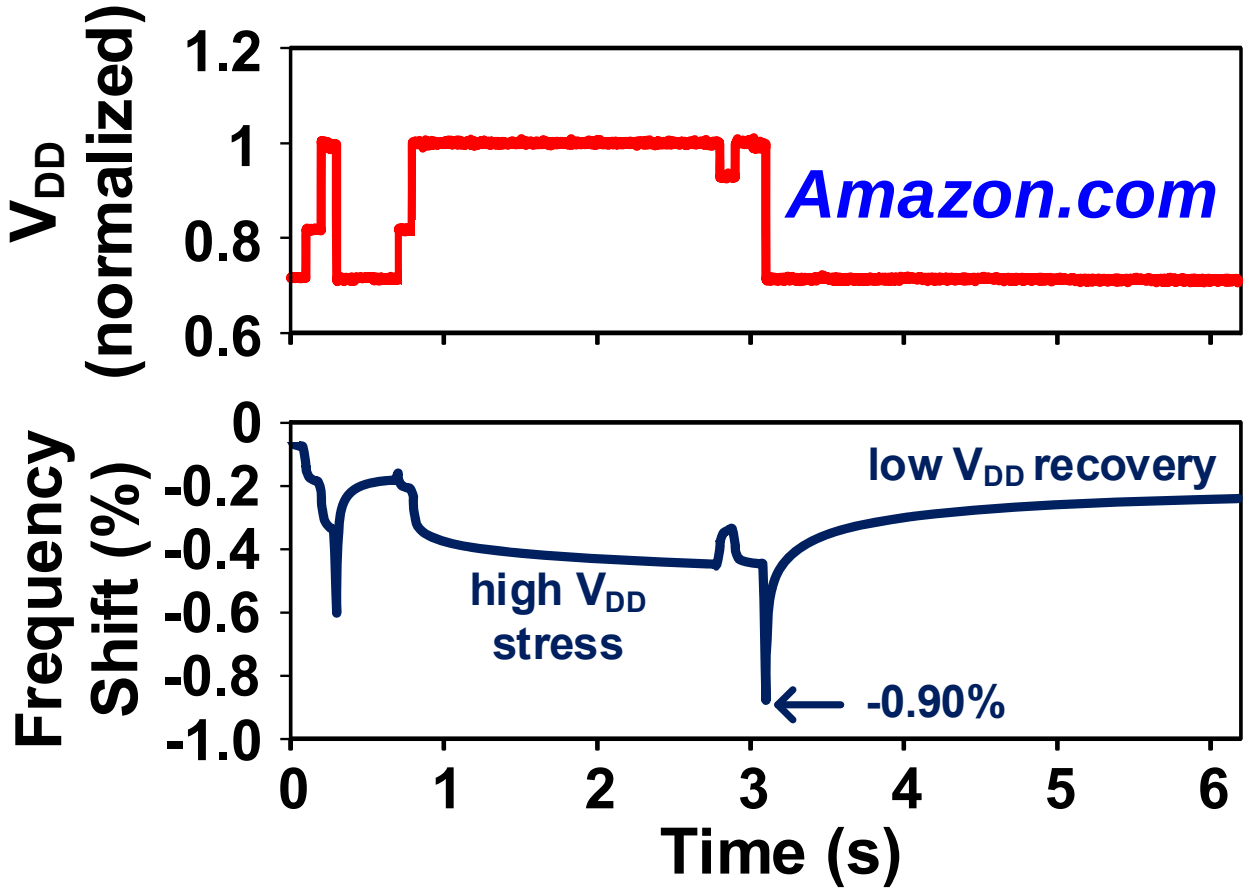
Android Development Board for Collecting DVFS Traces



Processor	ARM Cortex A15
System	Samsung Exynos 5410 SoC
Process	28nm
Frequency	0.8 – 1.8 GHz
Voltage	0.9 – 1.25 V
DVFS meas.	National Instr. DAQ
Sampling frequency	1000 samples per second
Linux kernel	v 3.4.5
Operating system	Android v 4.2.2

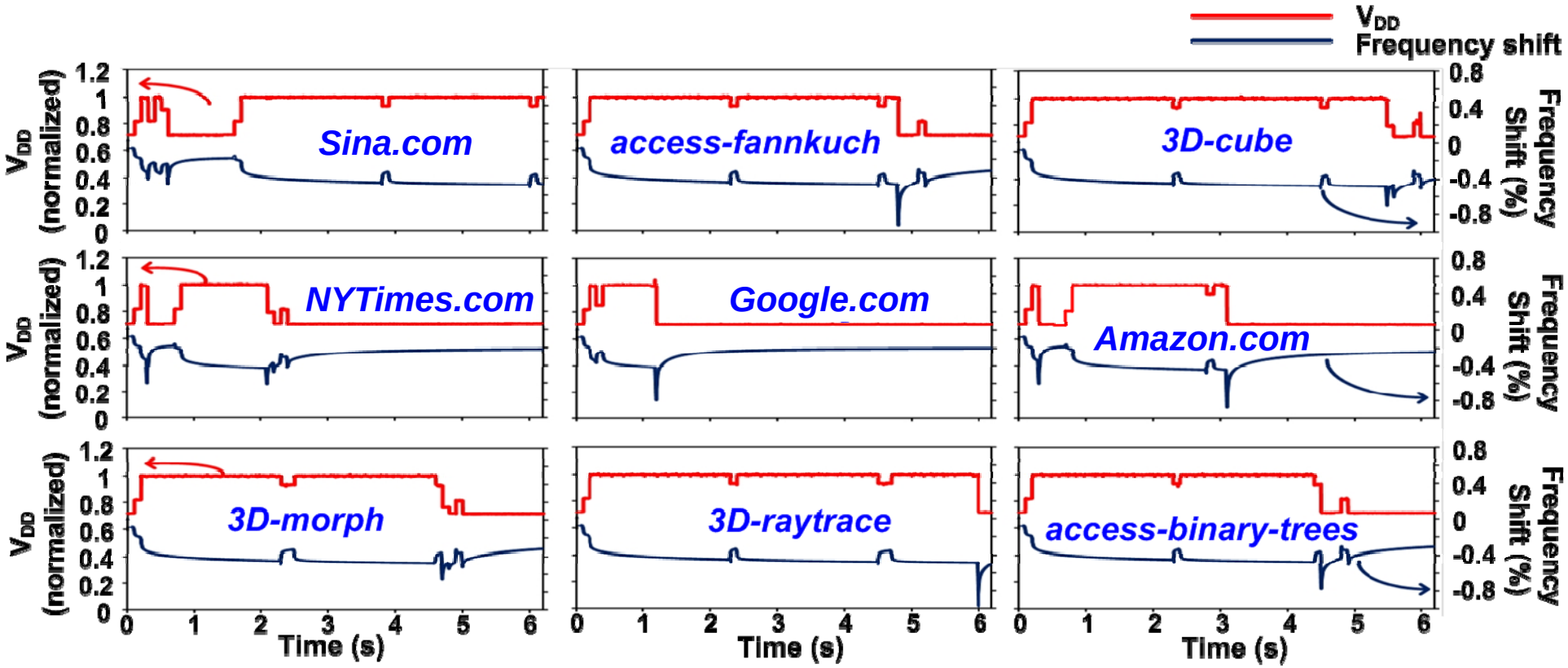
- V_{DD} and operating frequency collected in real time
- Navigating websites, running benchmark applications

Sample Waveform and Estimated Frequency Shift



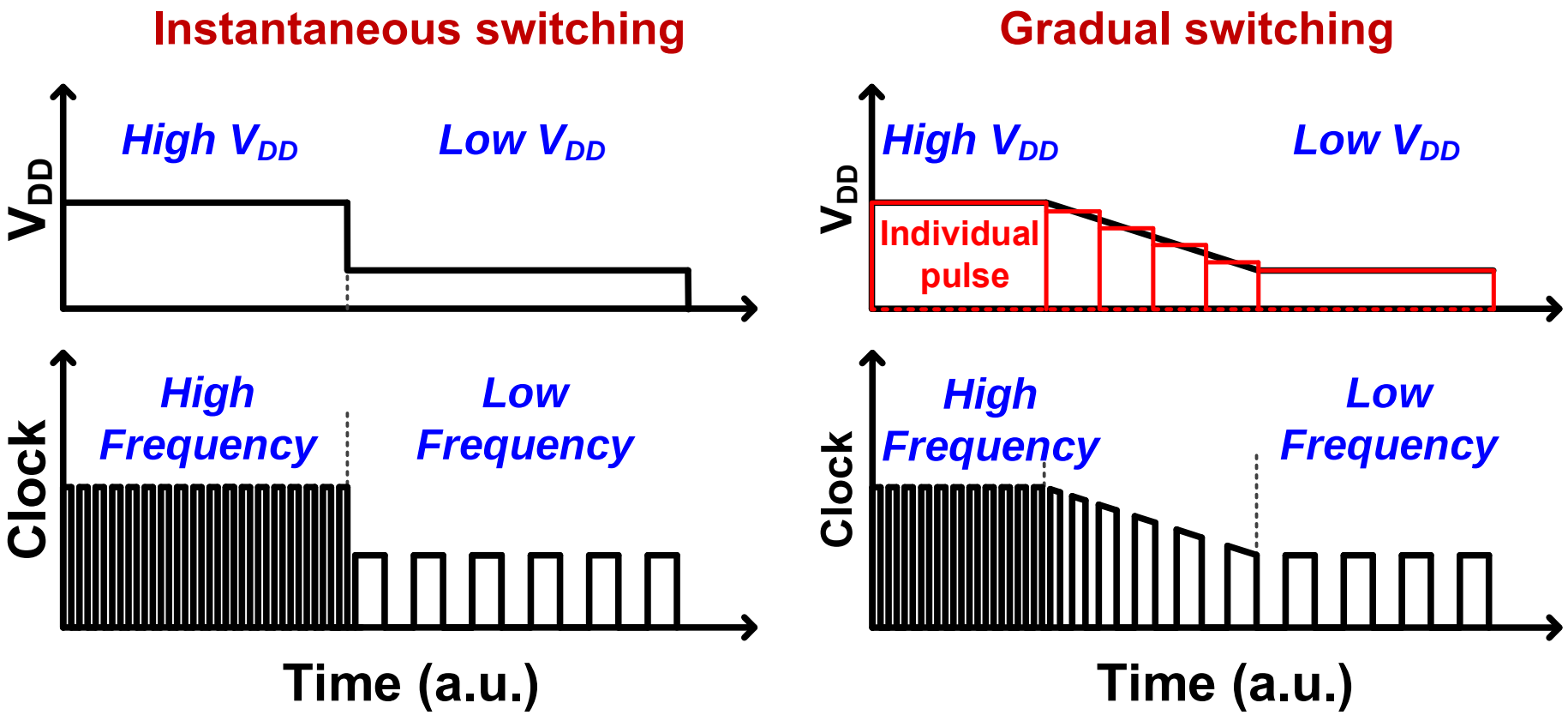
- High V_{DD} duration: Freq. degrades with time
- Low V_{DD} duration: Freq. shift dips and then recovers

Applying Model to Other DVFS Traces



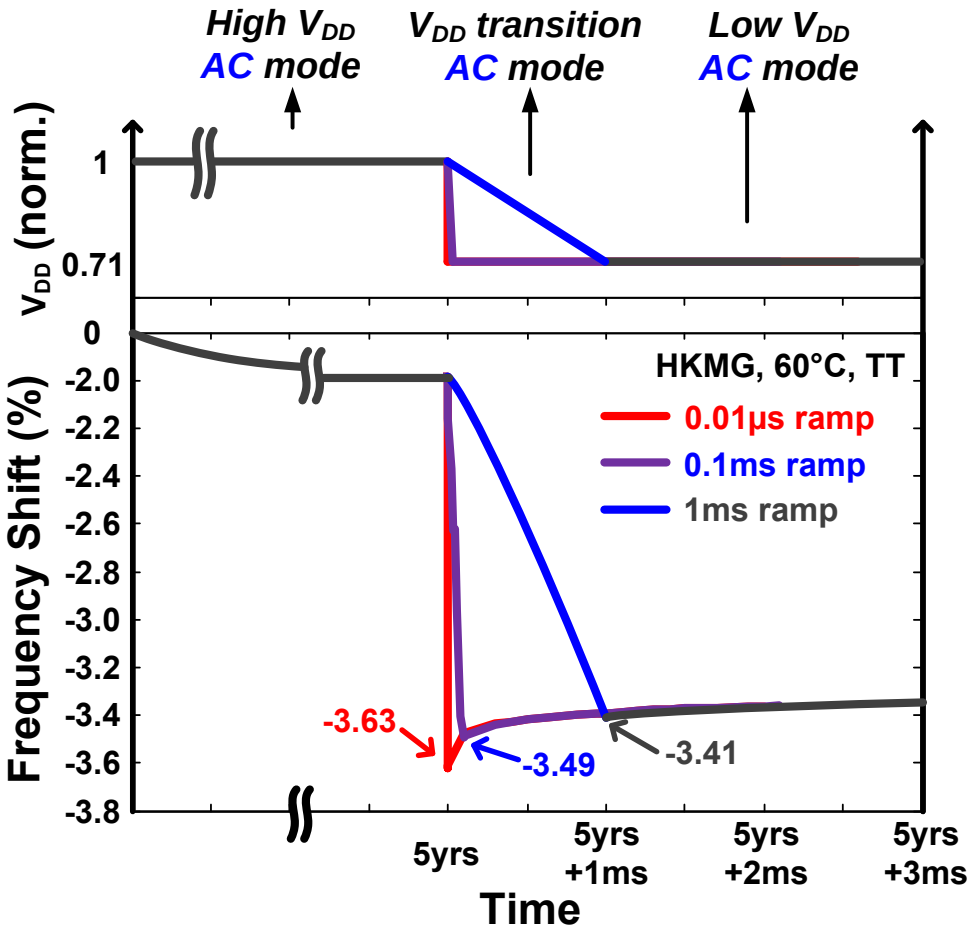
- **Worst case frequency dip**
  - **3D-raytrace: Δf=1.0% at t=6s when V_{DD} drops by 29% after staying in high V_{DD} mode for 5.8s**

Dependence on Transition Time



- Ramp voltage can be approximated as individual pulses with different heights
- Our empirical model can used to study the impact of ramp time on frequency shift dips

Ramp Time vs. Frequency Shift Dip



- **Ramp time: 0.01µs to 1ms → Δf dip: -3.63% to -3.41%**
- **Explanation: Recovery kicks in before lowest V_{DD} reached**

Summary

- An empirical BTI model for DVFS analysis developed
  - A recovery model is derived from R-D stress model using superposition property
  - Capable of handling complicated DVFS scenarios
  - Short simulation time (< 1 minute using Matlab)
- BTI induced frequency degradation estimated for the first time using real DVFS traces
  - V_{DD} traces for various benchmarks collected from an ARM Cortex A15 processor
  - Frequency shift dips and peaks are estimated using proposed empirical model