Amdahl's Law in Big Data Analytics: Alive and Kicking in TPCx-BB (BigBench)

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February 28, 2018



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Big data analytics deals with data sets **too large**, problems **too complex**, and patterns **too subtle** to be handled by conventional relational databases.





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CloudSuite

BigDataBench

AMPLab Benchmarks

LinkBench

YCSB

DCBench

HiBench



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What is it and why should computer architects care?

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BigBench was standardized as TPCx-BB in 2014.

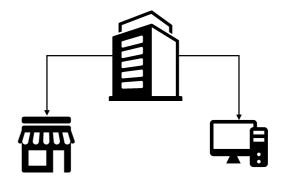




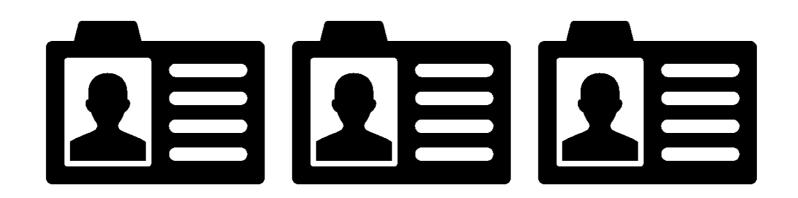
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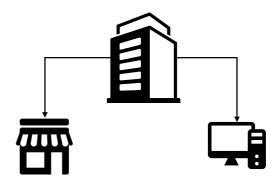




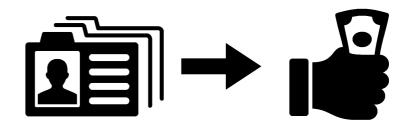
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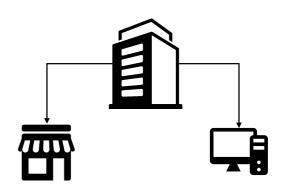


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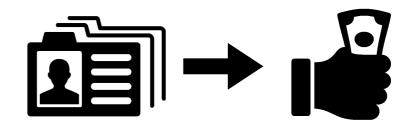
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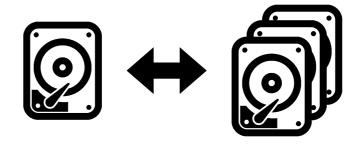
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Data size is configurable from 1 TB to 1 PB.













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Most queries take multiple steps, and many cover multiple data types and operation types.



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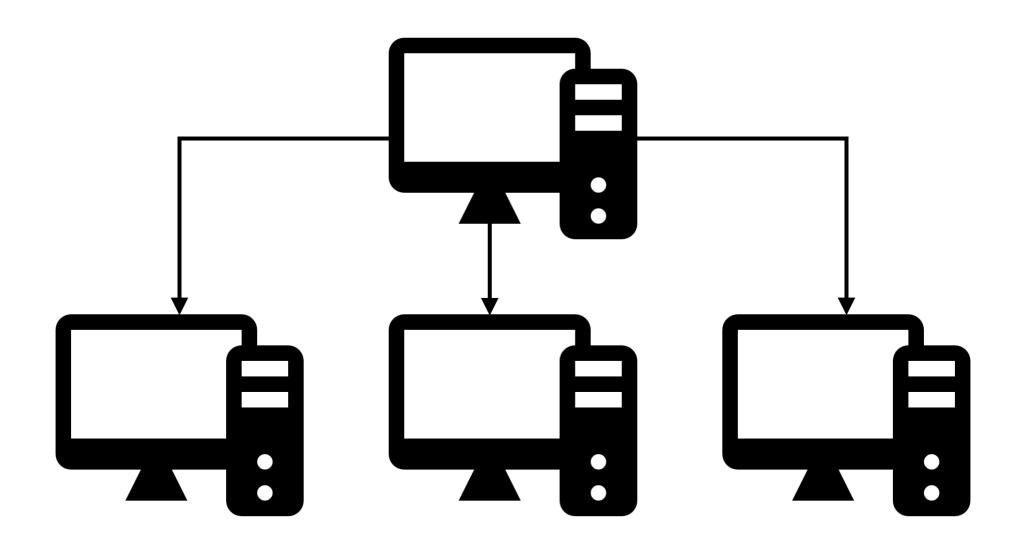
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Thread-limited execution is still pervasive even in scale-out big data analytics and demands better scale-up performance (Amdahl's law).



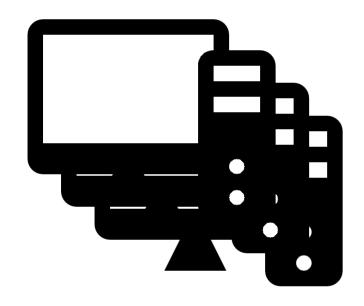


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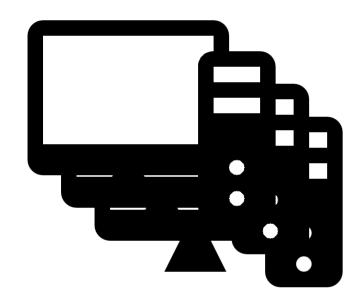
Intel Xeon E5-2699 v3

384 GB RAM

SSD Storage



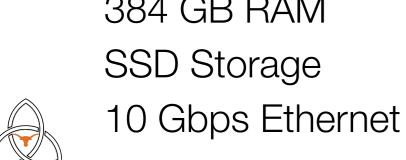
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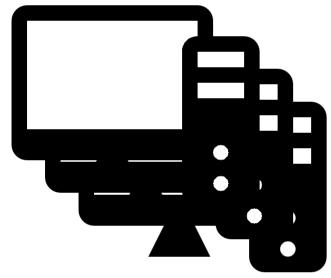
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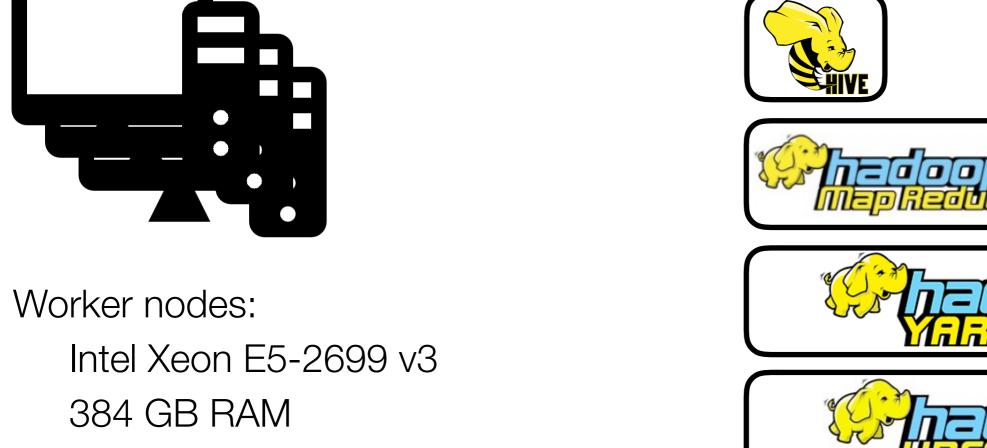




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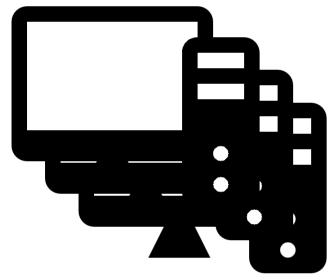


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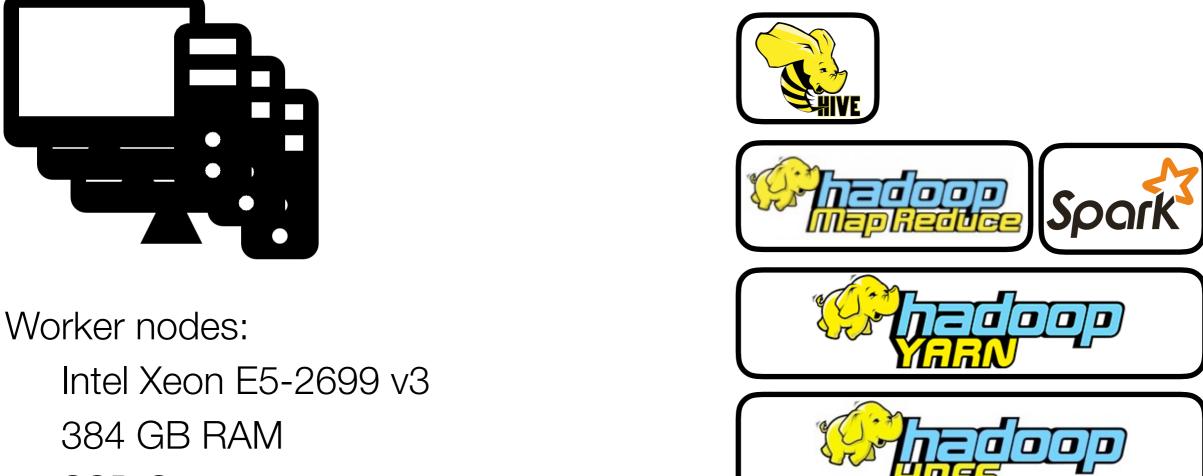




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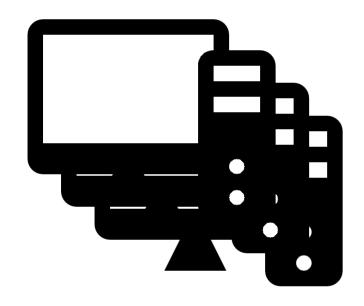


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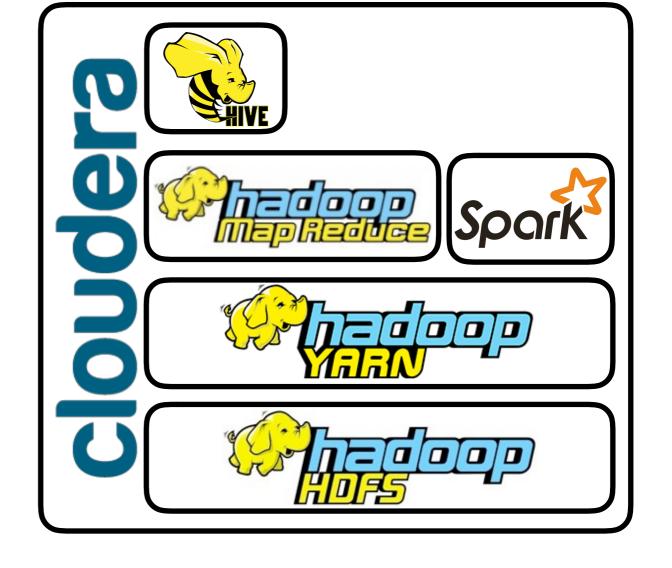
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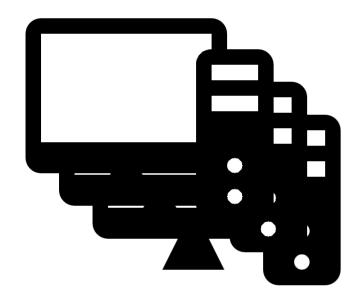






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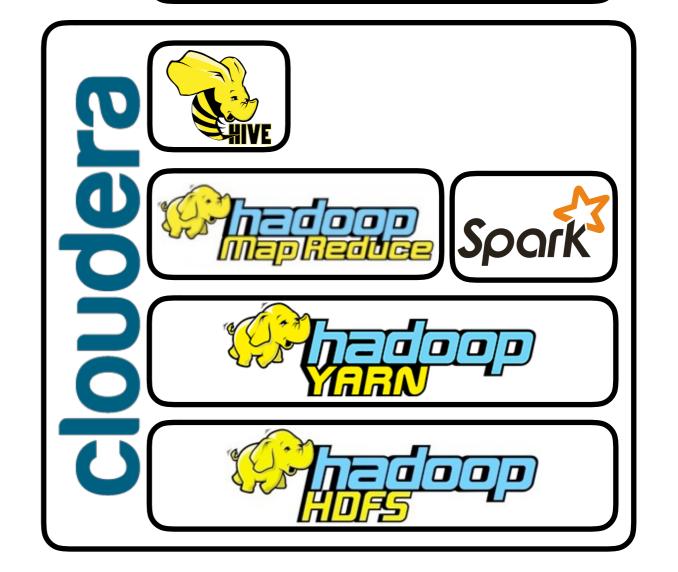


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Creates the data used by the benchmark.



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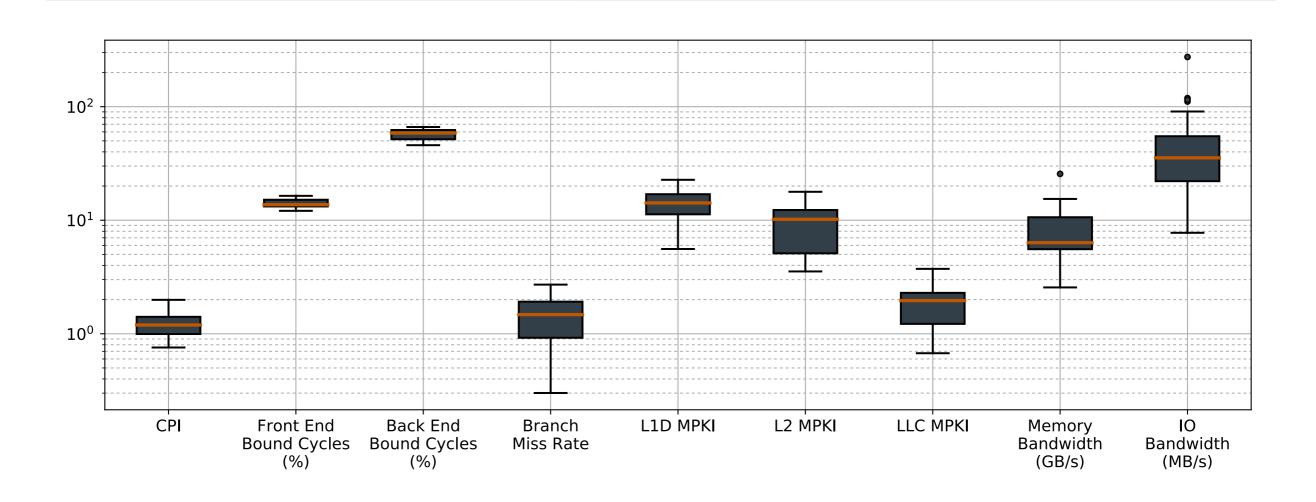
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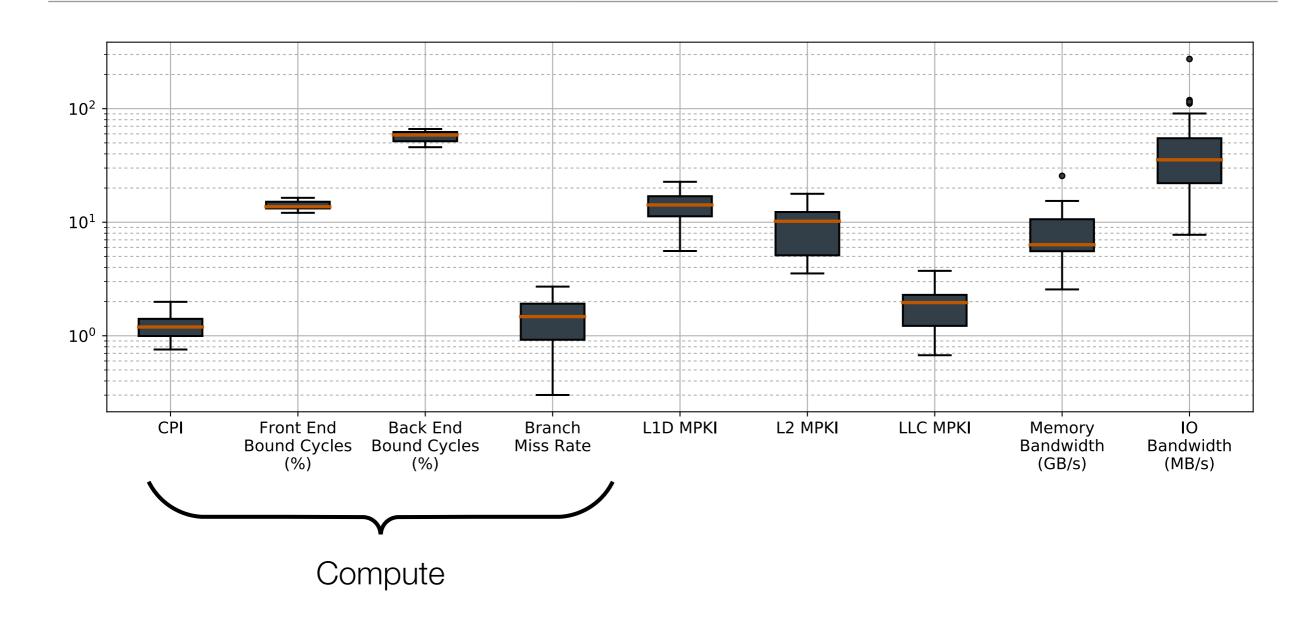




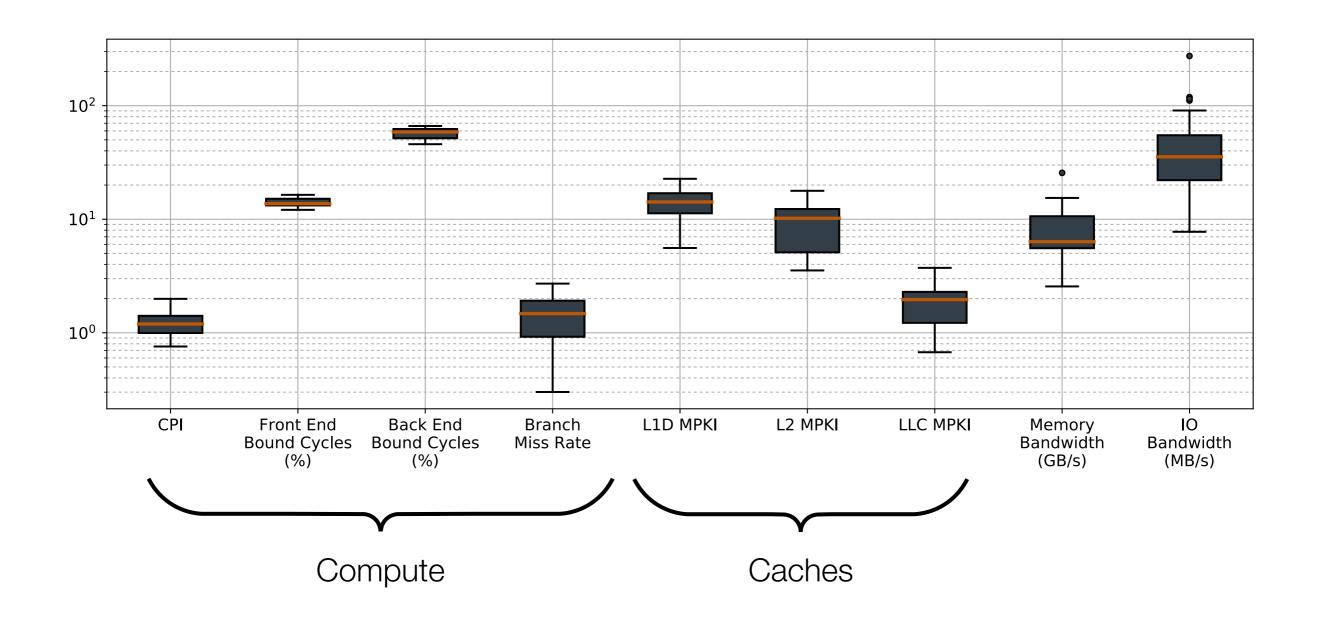




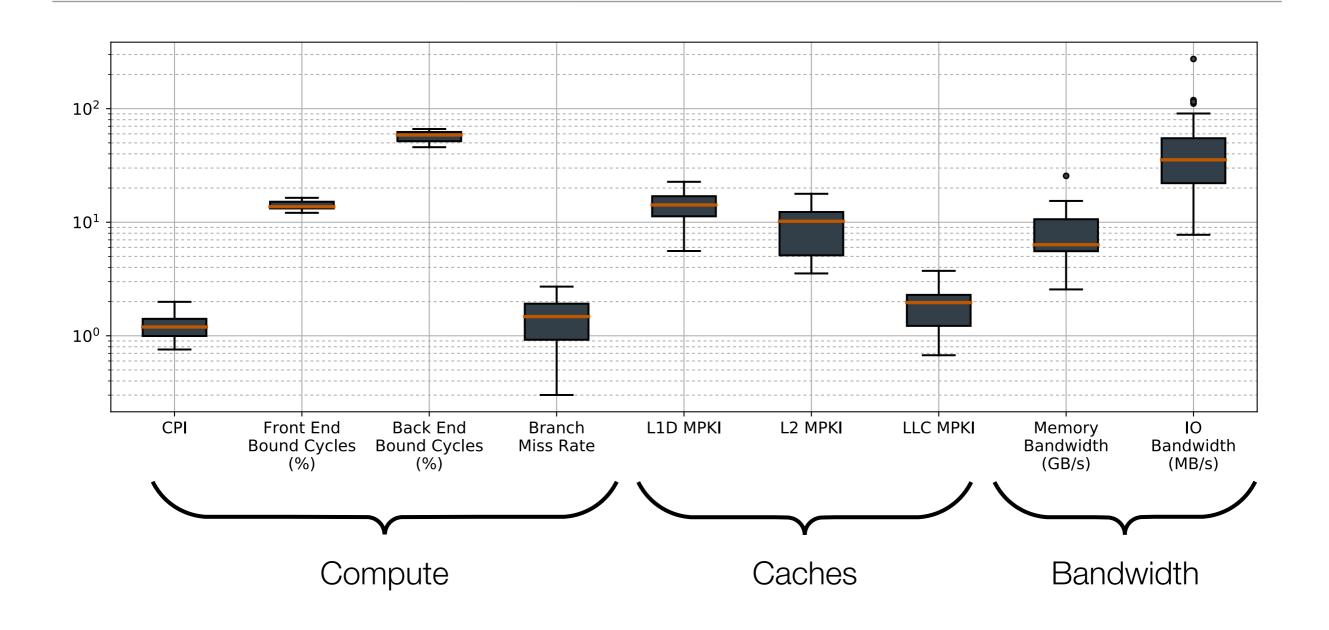




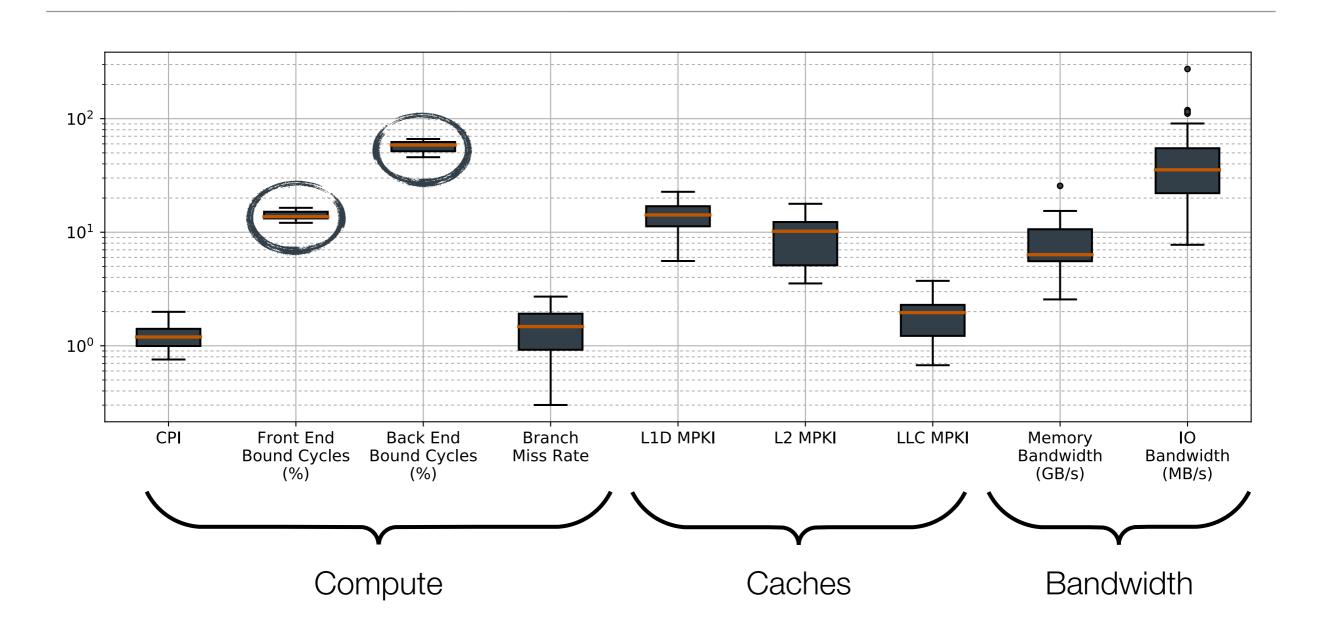






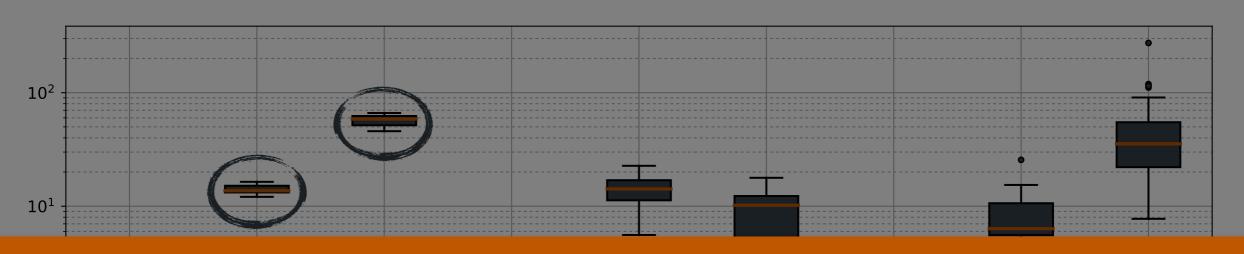




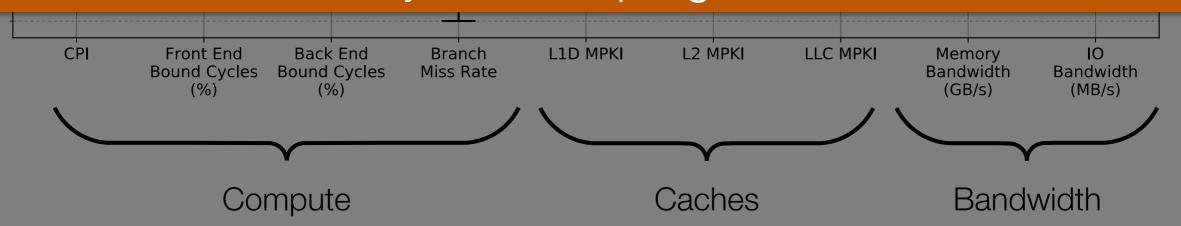


Only the front and back end-bound cycles are stable across queries.





Big Data Analytics applications are too varied to represent with just a few programs.



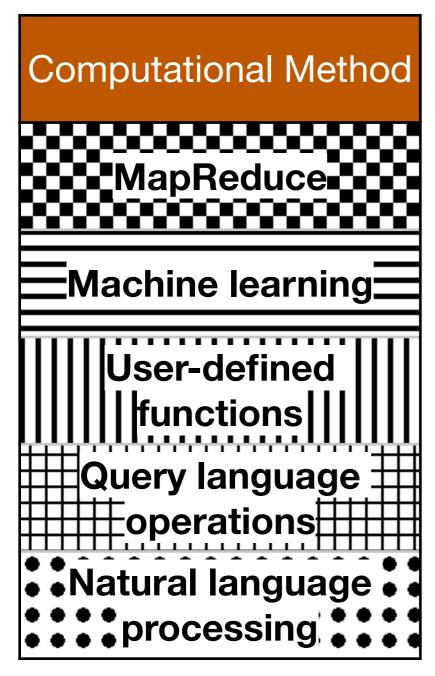
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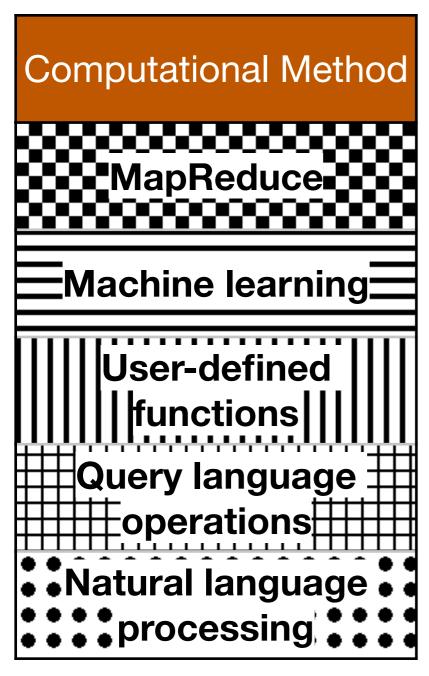


Computational Method



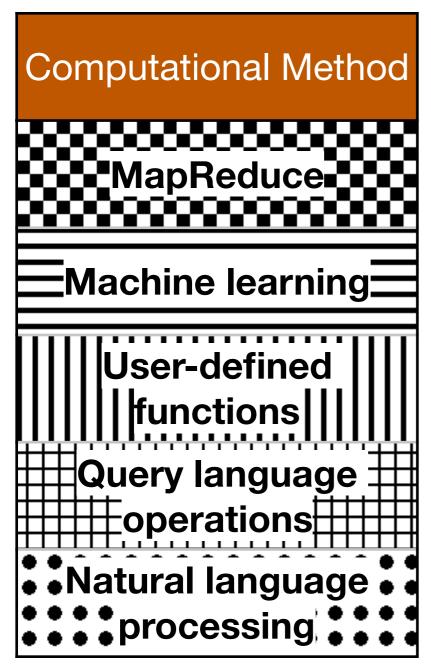






Data Type





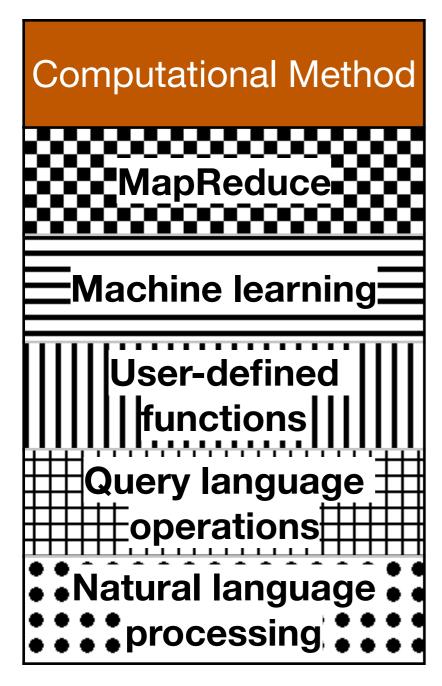
Structured

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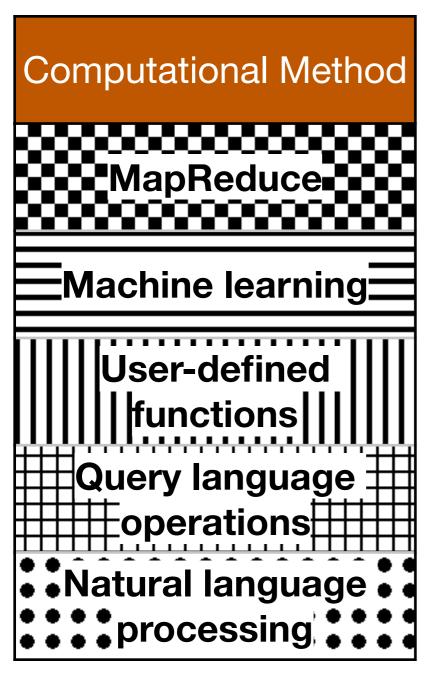
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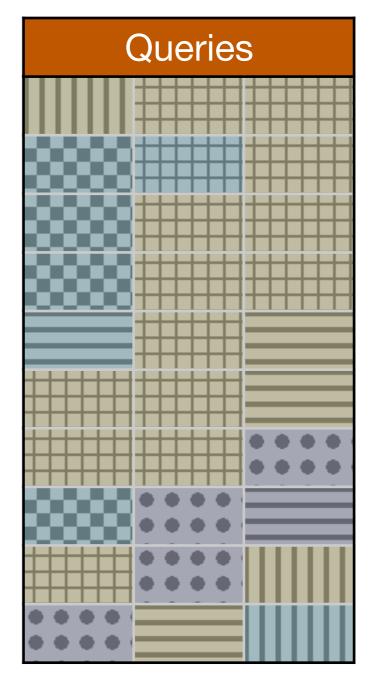


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Architecturally, the reason you're able to deal with lots of data is because Hadoop spreads it out...You've got all of these processors, working in parallel, harnessed together.



Cloudera Co-Founder Mike Olson



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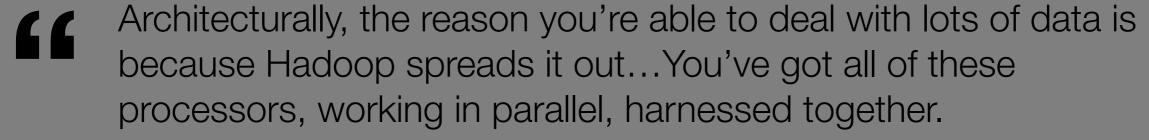
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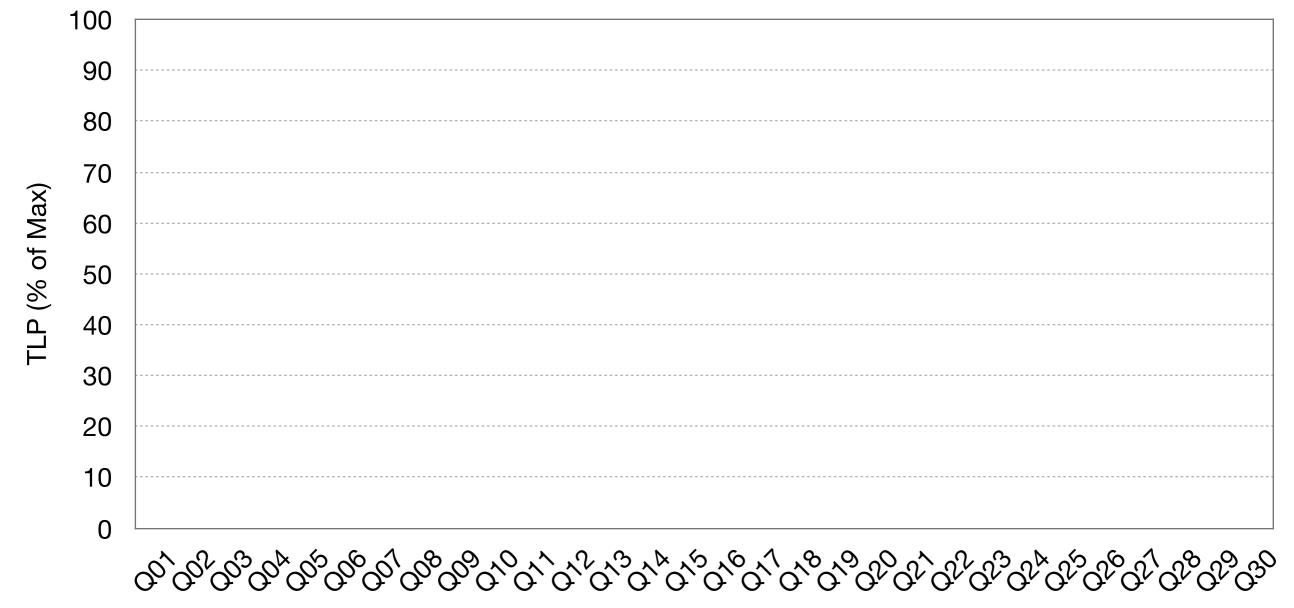




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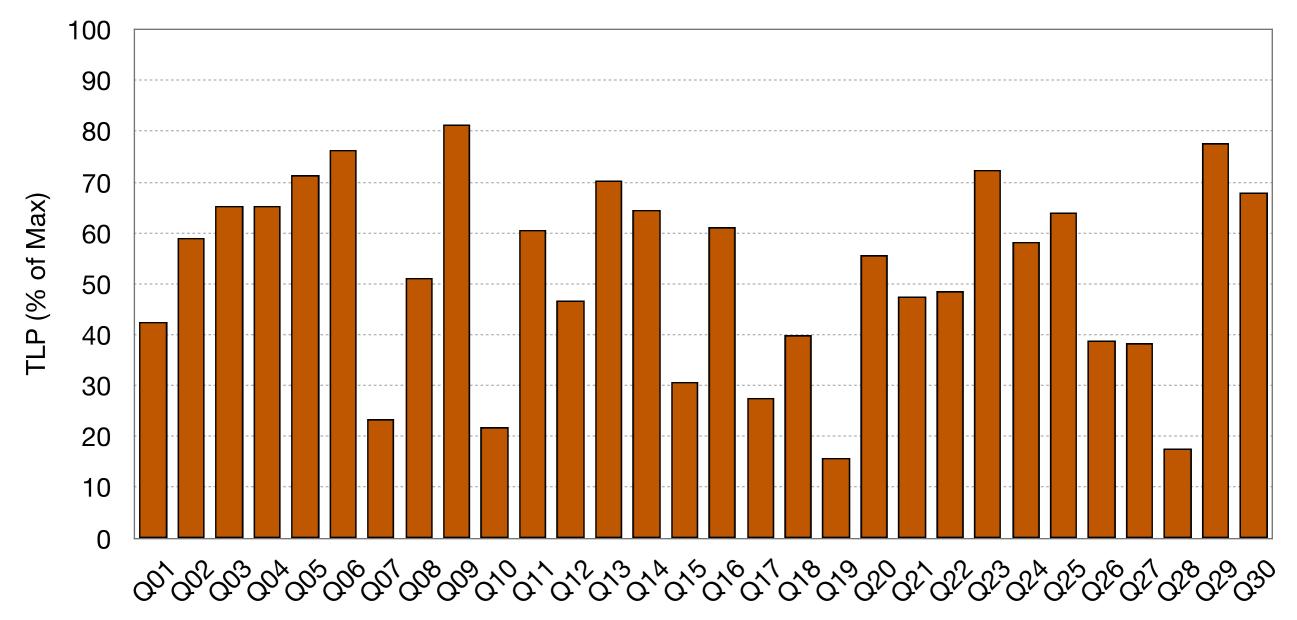




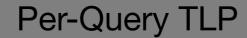


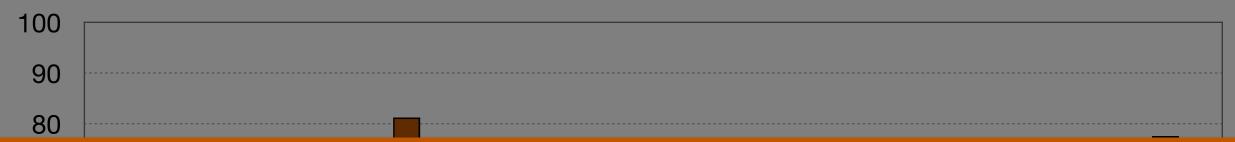




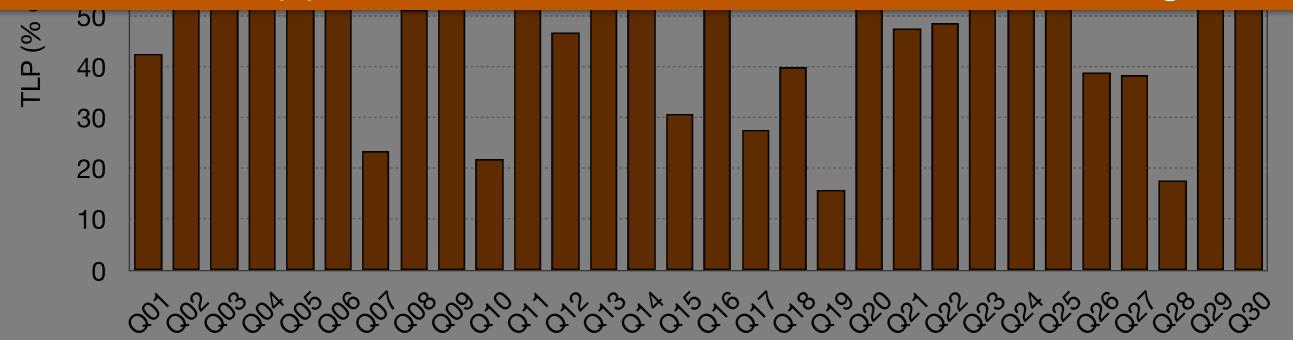








Despite common wisdom that big data is perfect for scale-out, these applications show universal TLP shortcomings.







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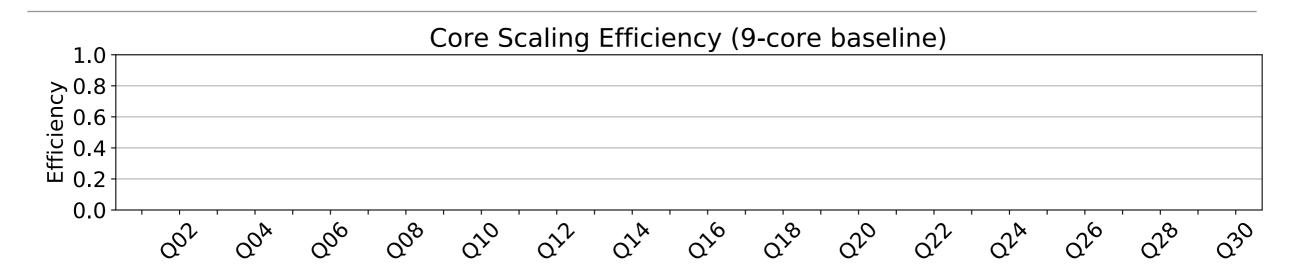


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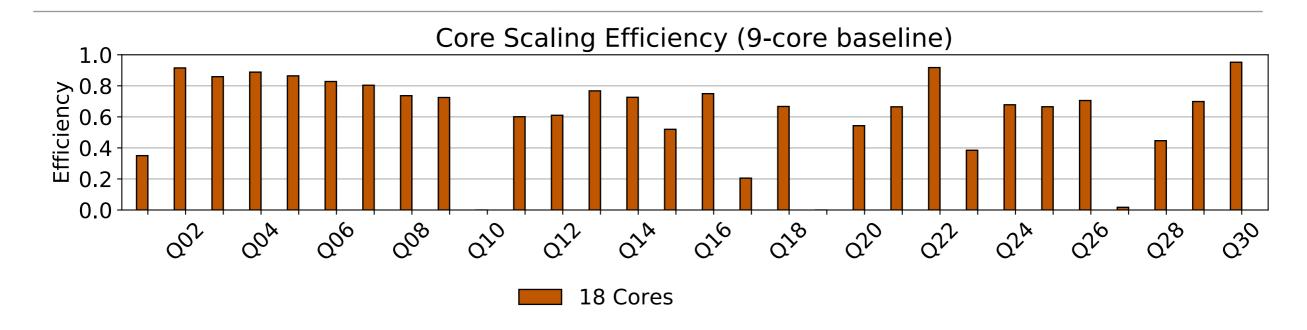
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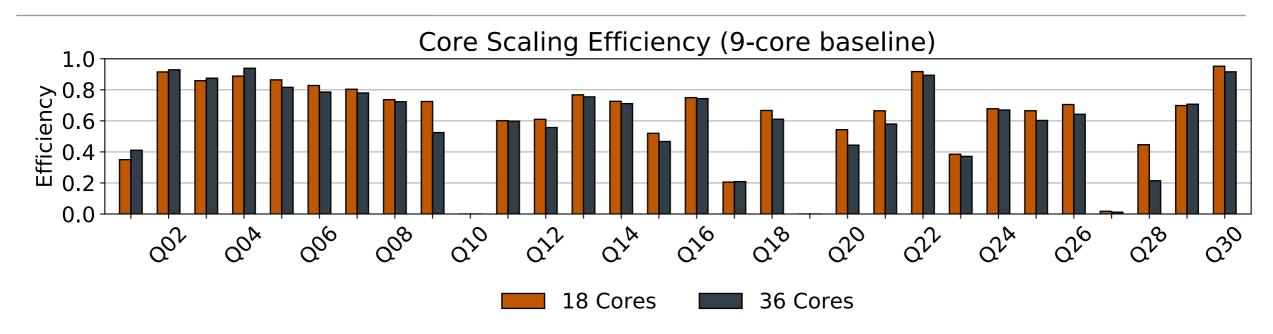




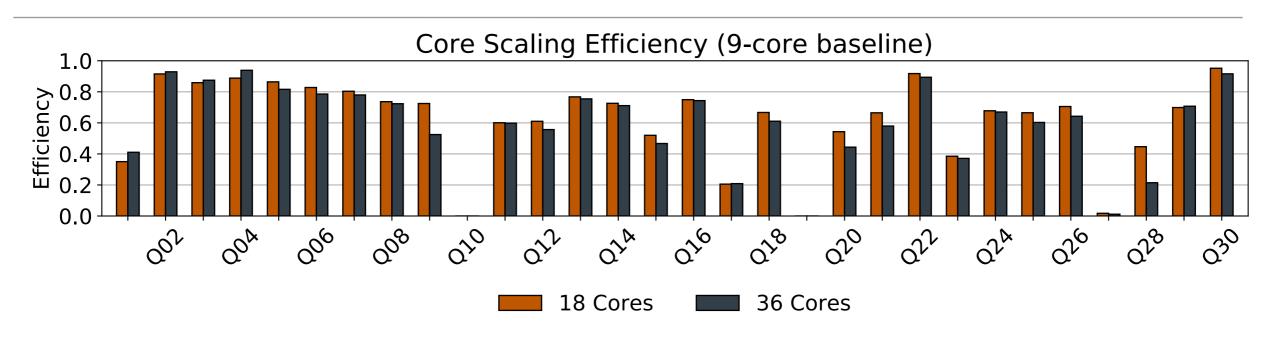


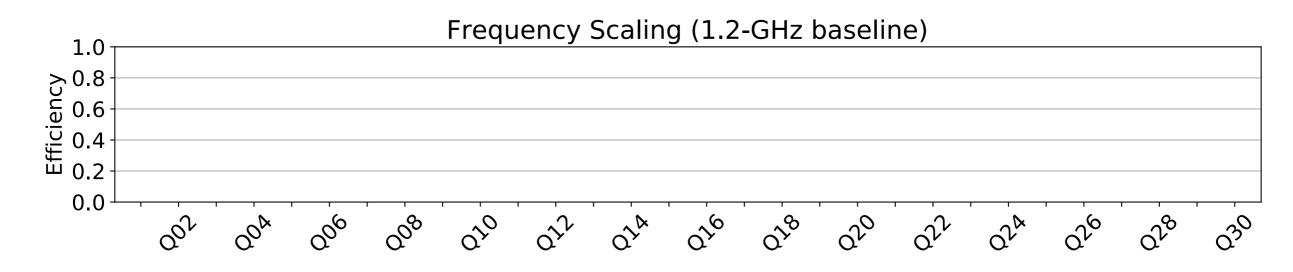




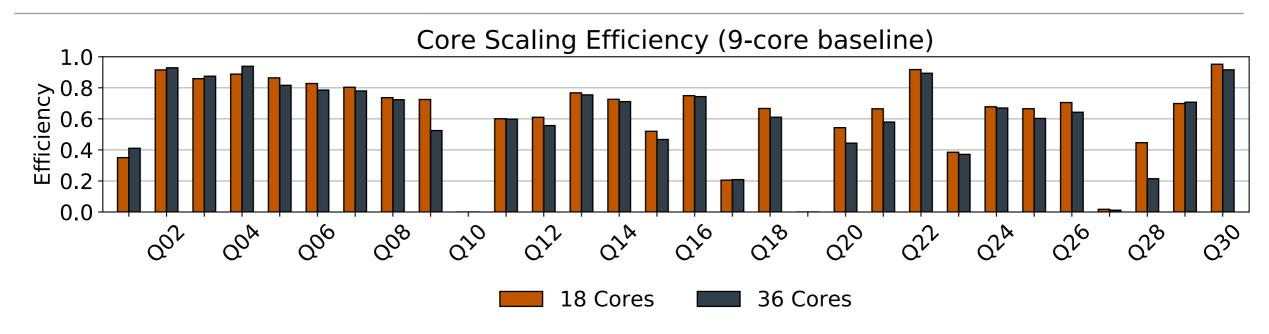


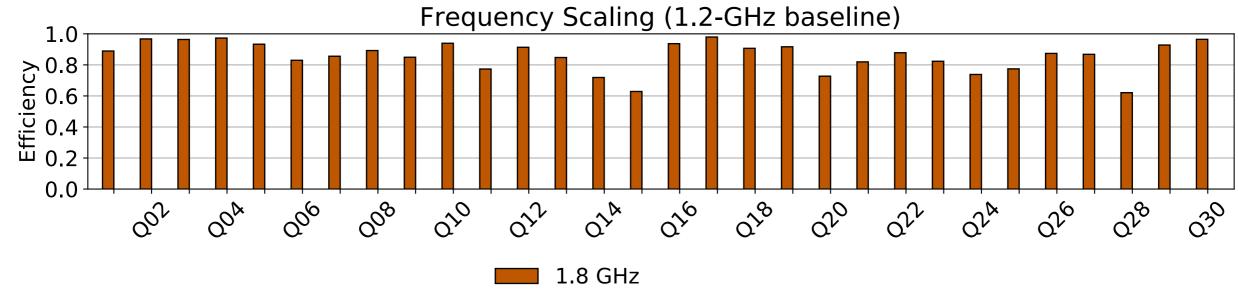




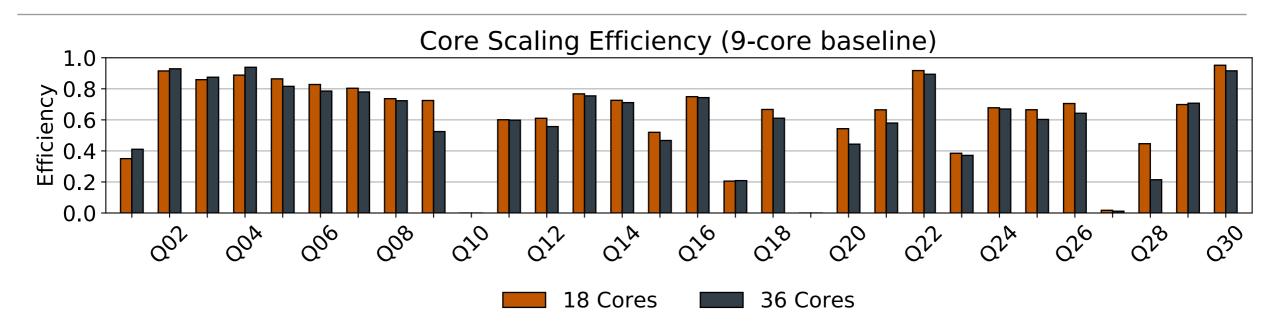


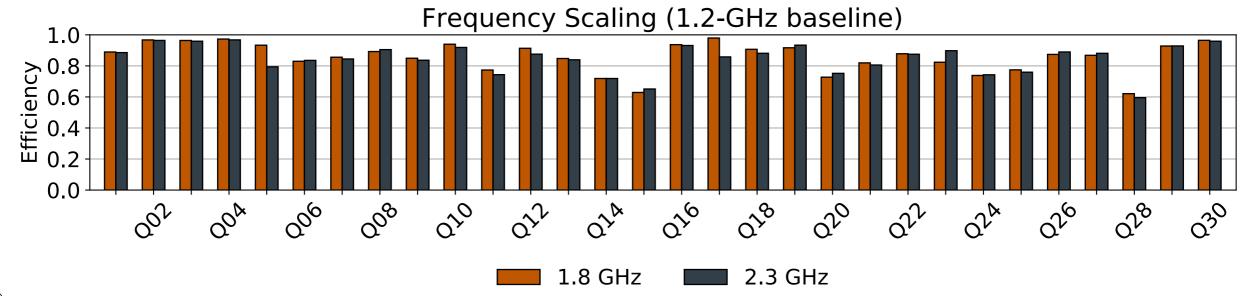




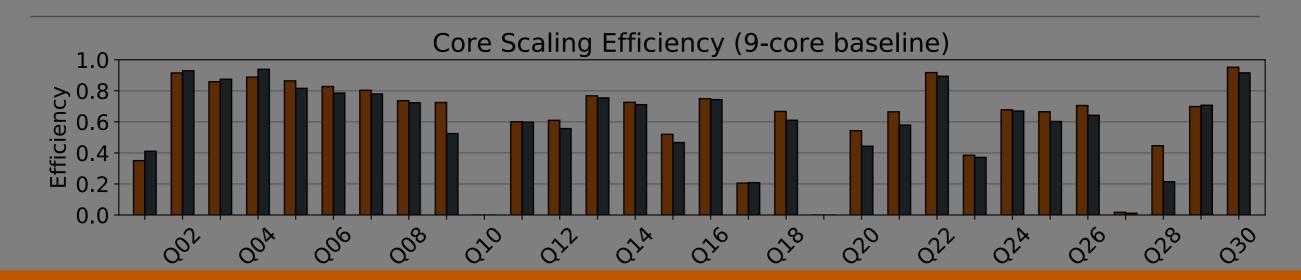




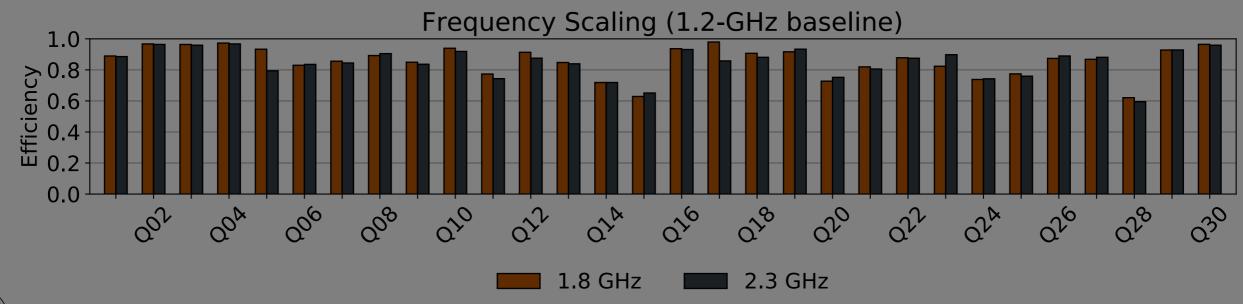








Frequency scaling is more efficient than core scaling.







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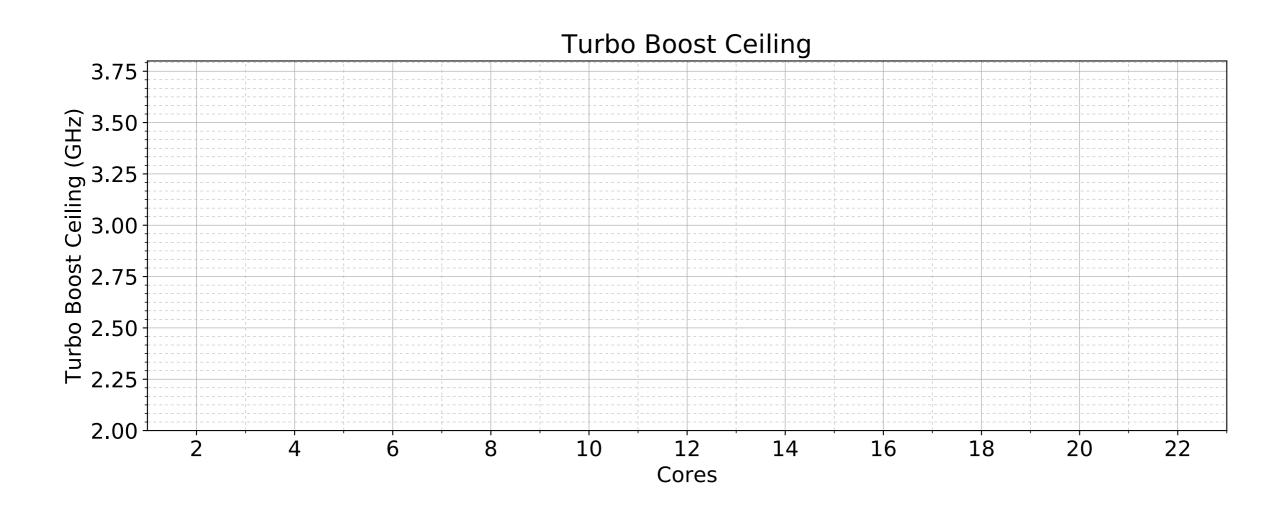
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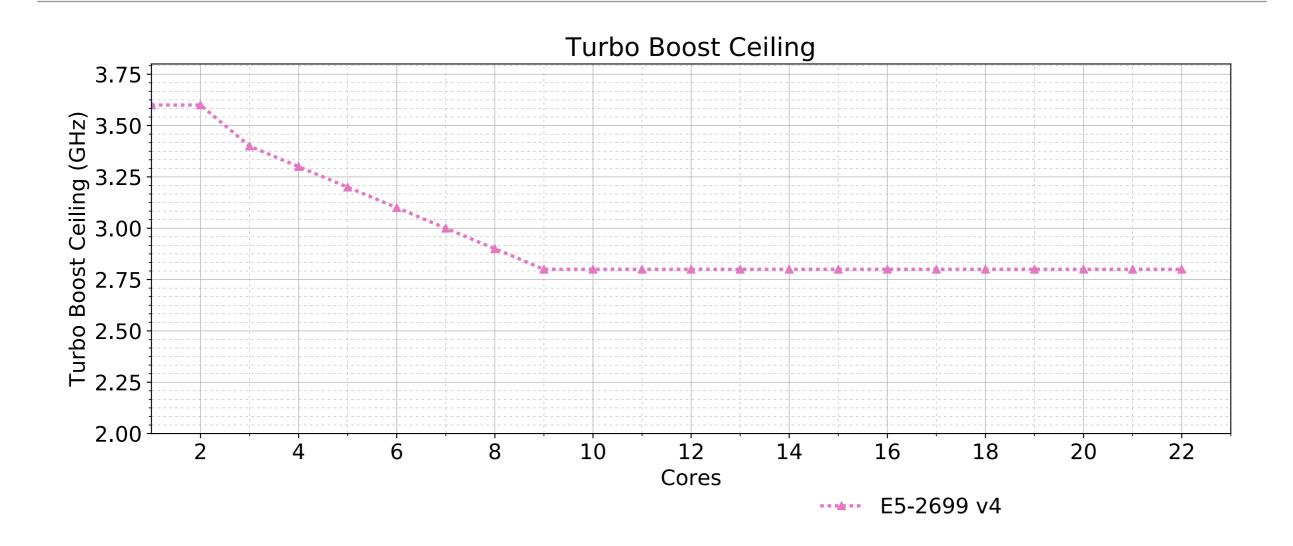
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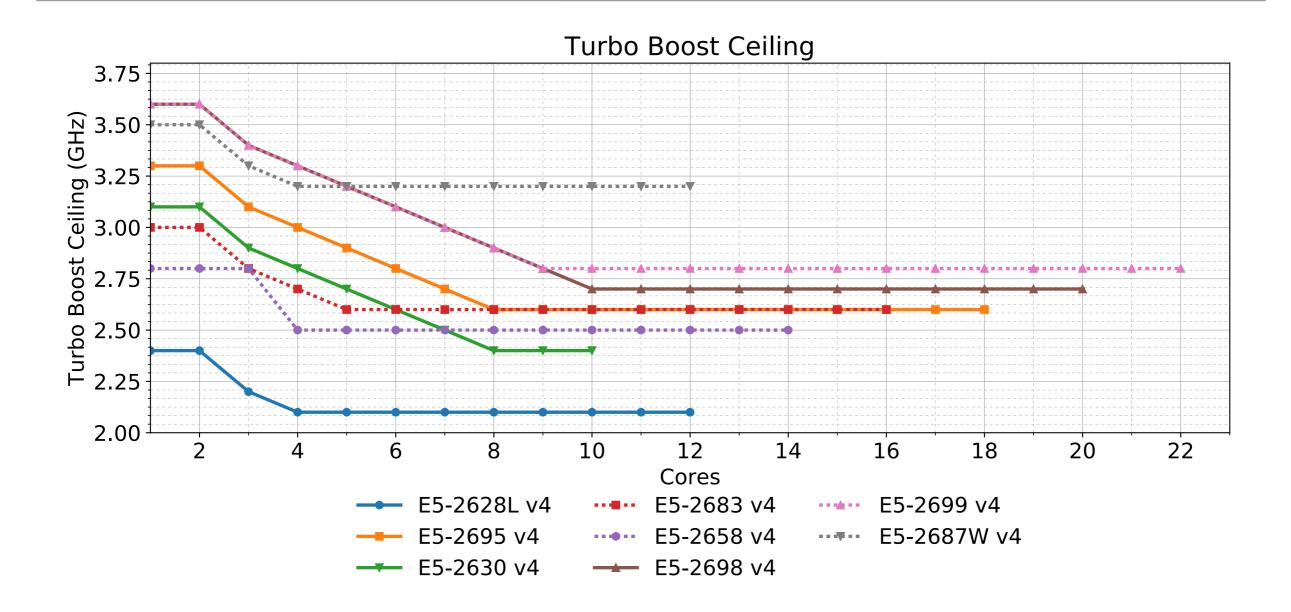




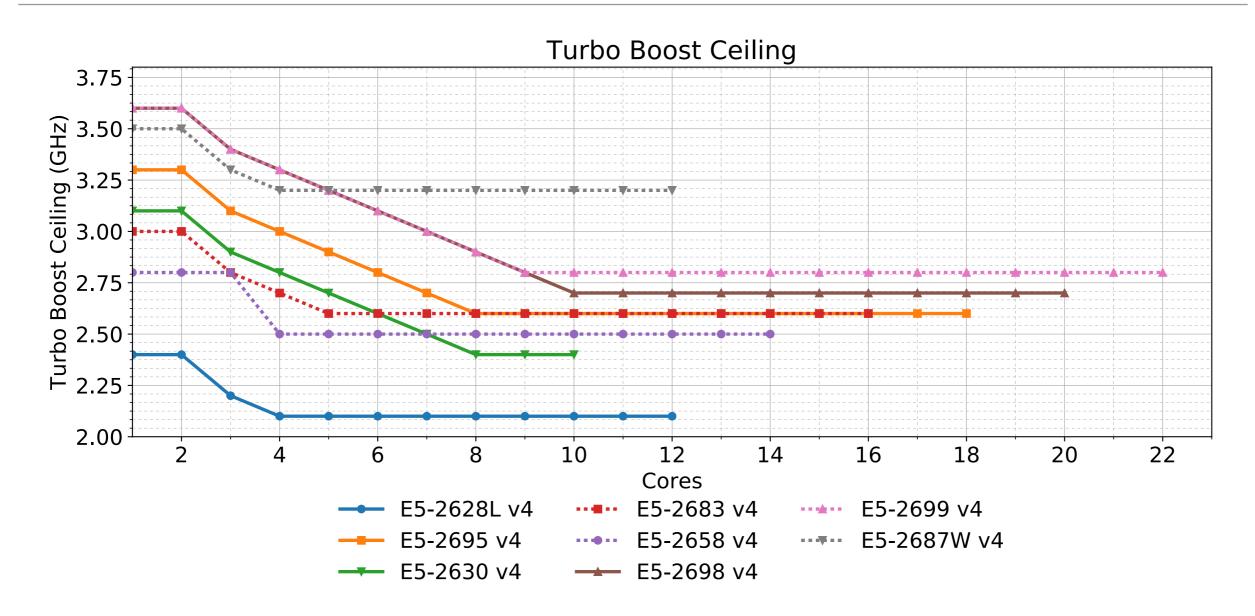






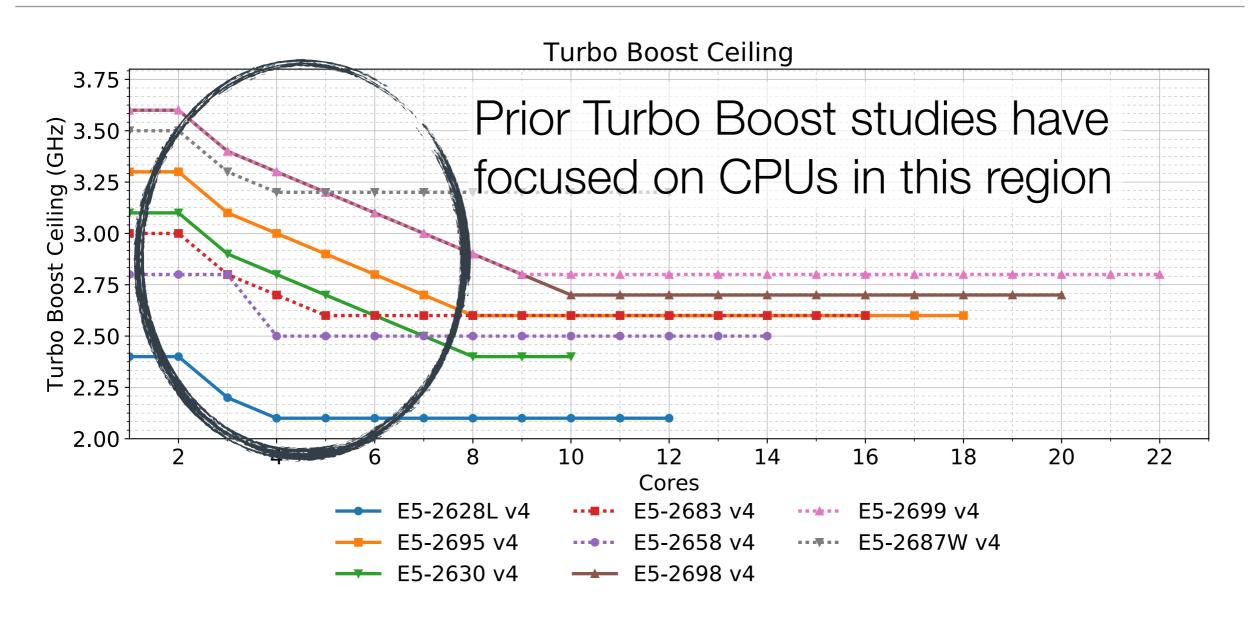






The Turbo Boost ceiling does not increase until most cores have been disabled.





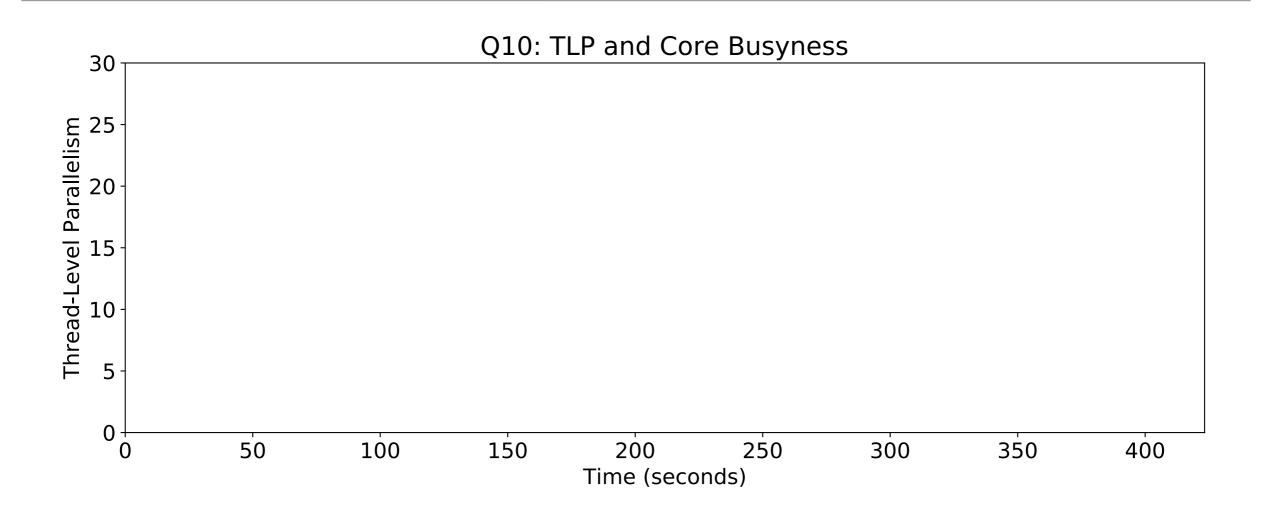
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A Deeper Problem...Compounded By Software

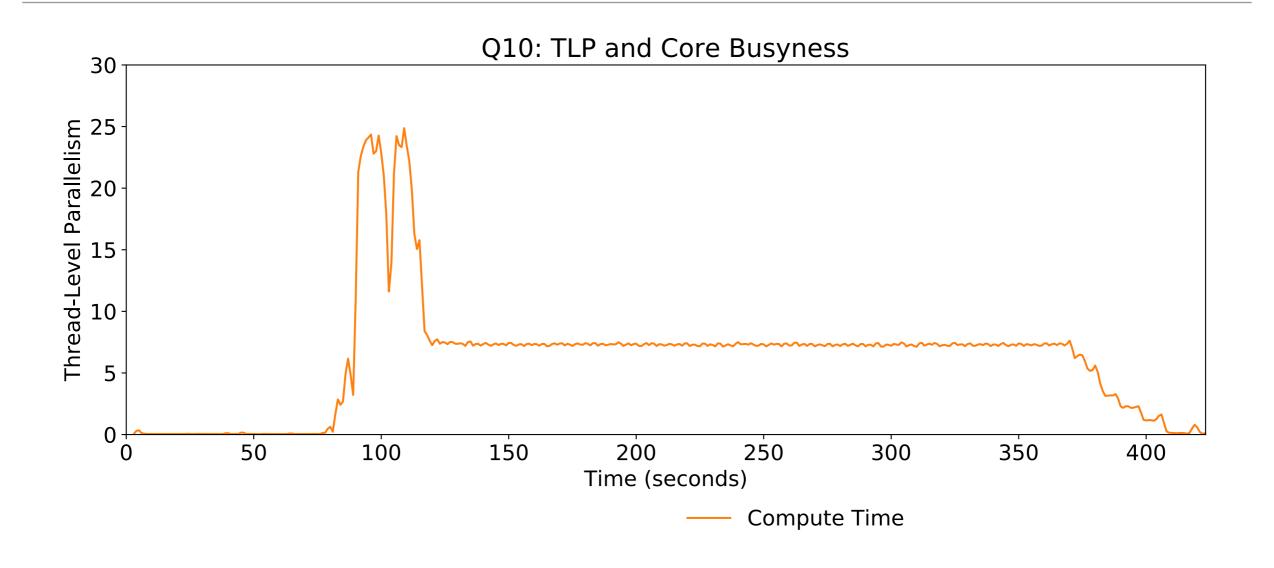


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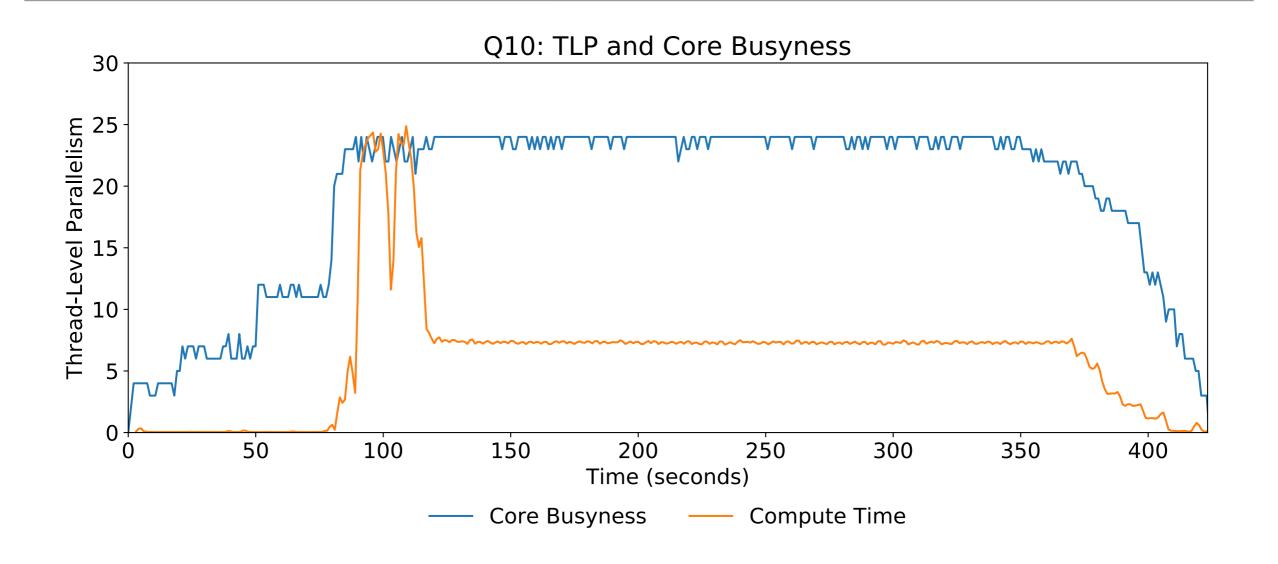


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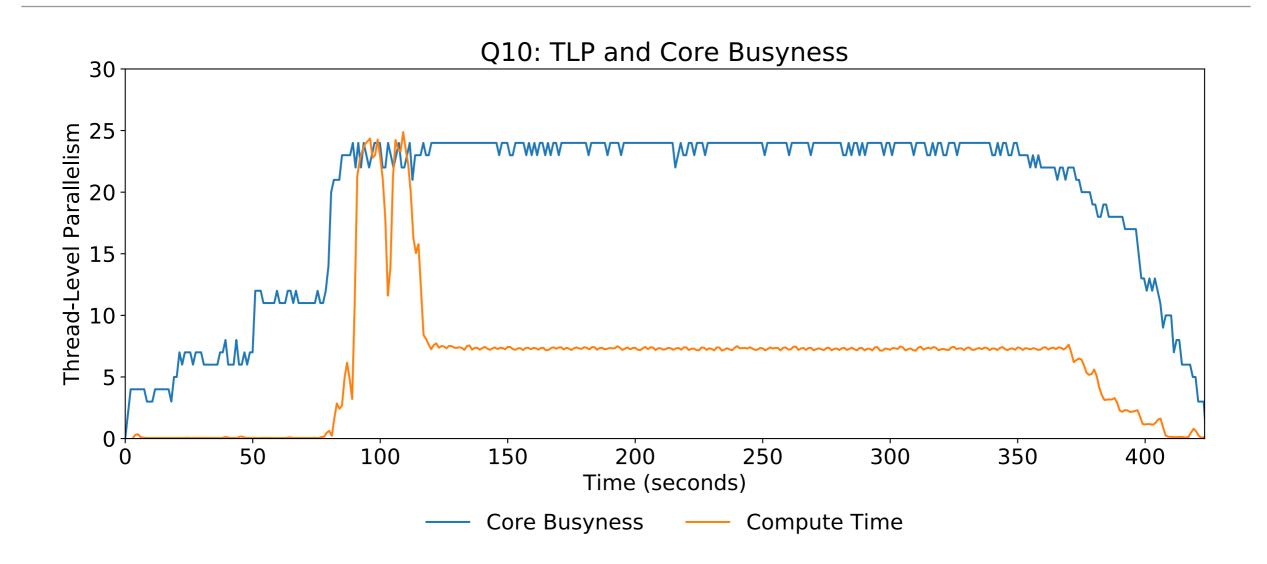


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Despite having very little TLP, nearly all the cores are kept busy most of the time.





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Software: The abundant software threads are being scheduled onto virtually all available cores, whether they are actually needed or not.



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Hardware and software cooperatively prevent

Turbo Boost from ever exceeding its baseline ceiling.

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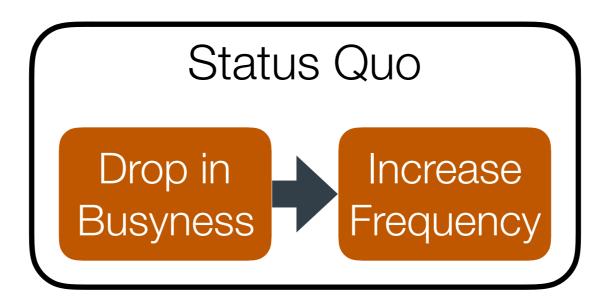




Core packing is our proposal for proactive enhancement of Turbo Boost through hardware and software cooperation.

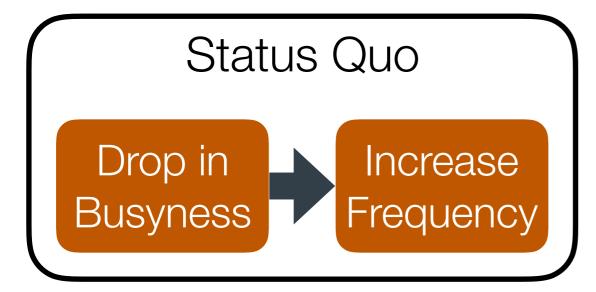
Status Quo





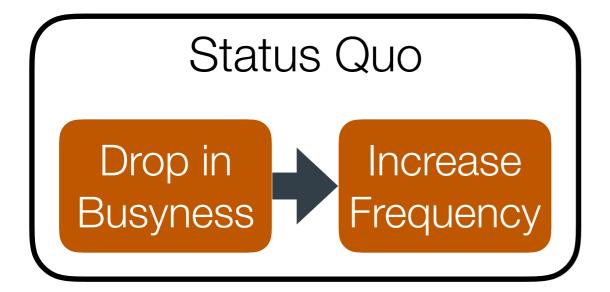


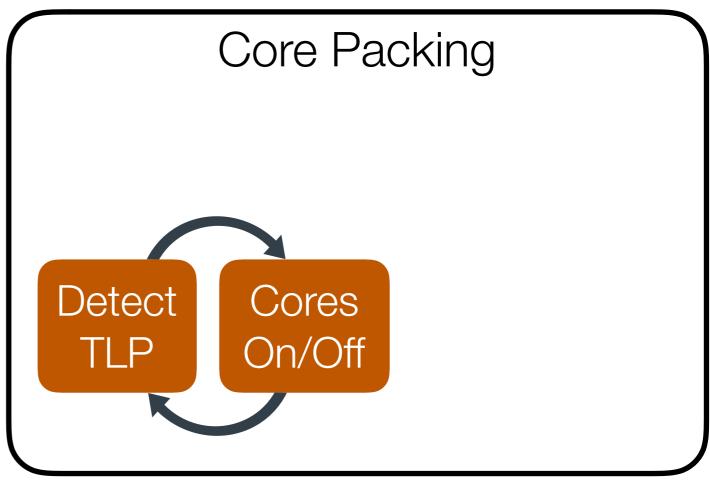
Core packing is our proposal for proactive enhancement of Turbo Boost through hardware and software cooperation.



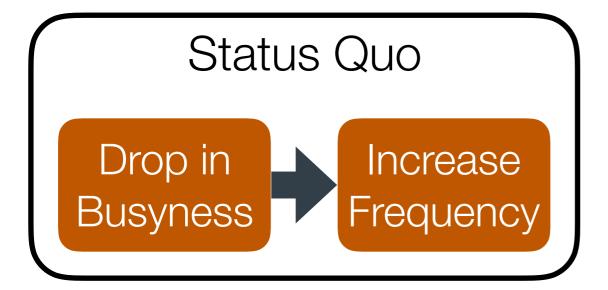
Core Packing

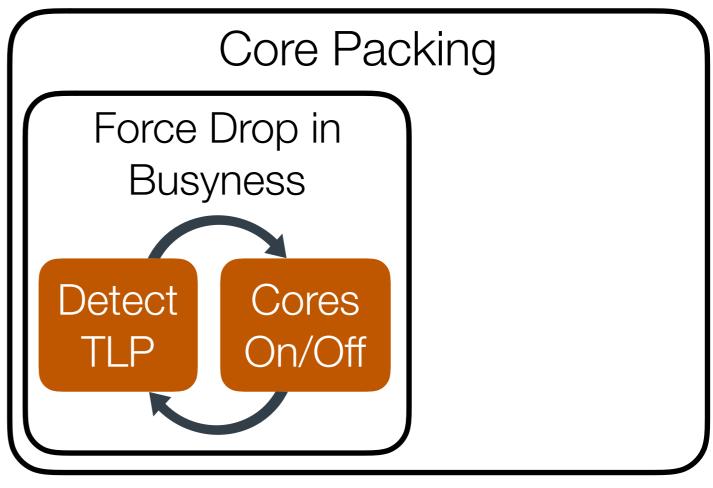




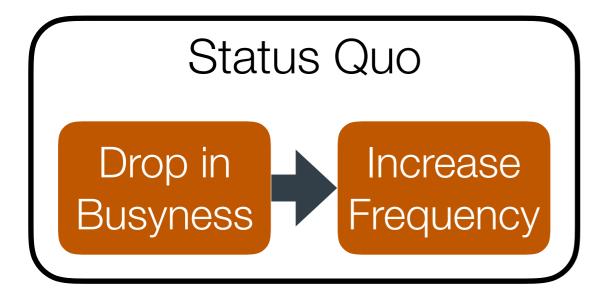


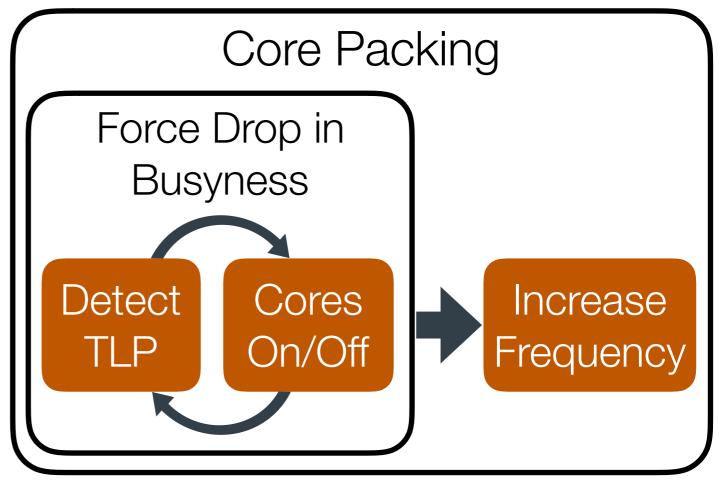












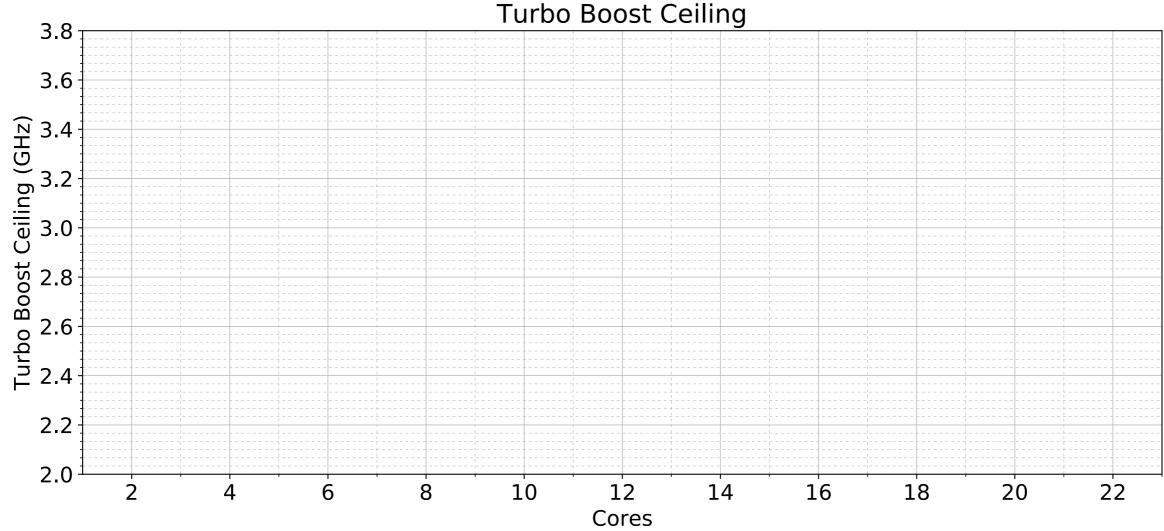




Allow for linear increase in Turbo Boost ceiling with the number of deactivated cores.

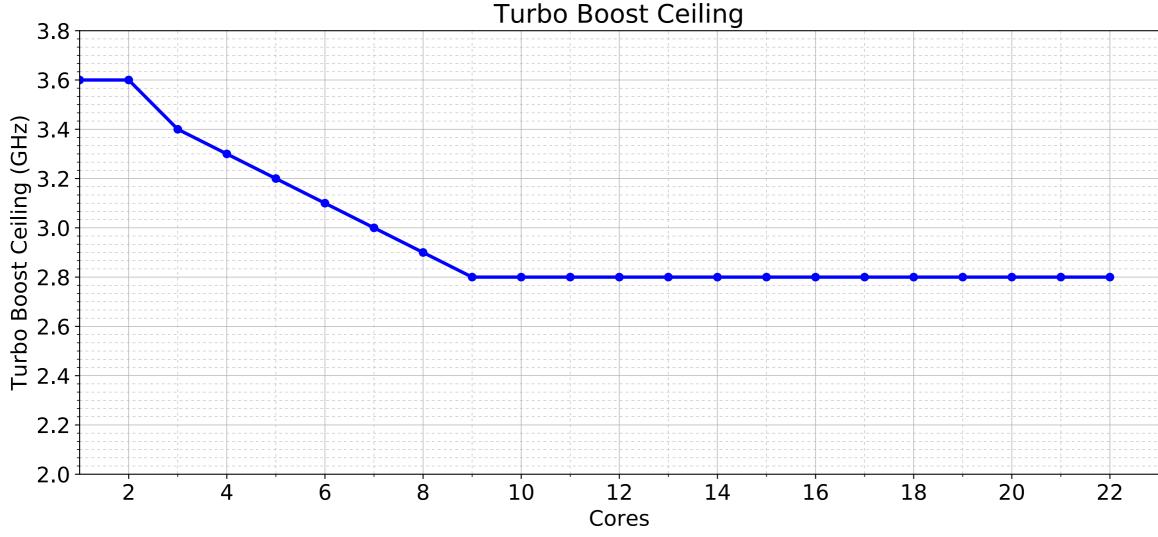


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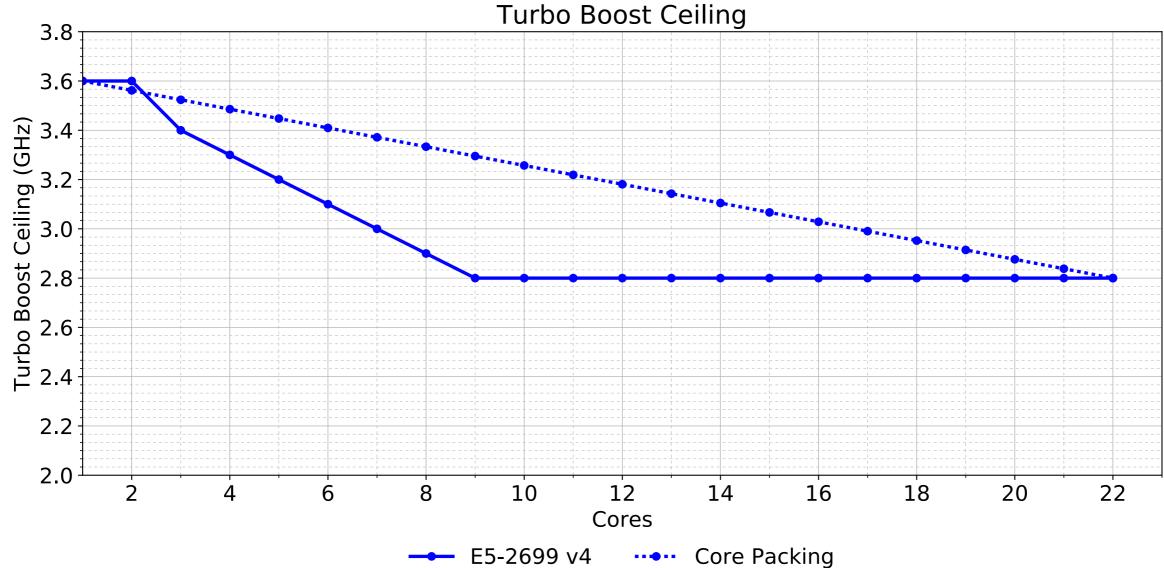
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E5-2699 v4



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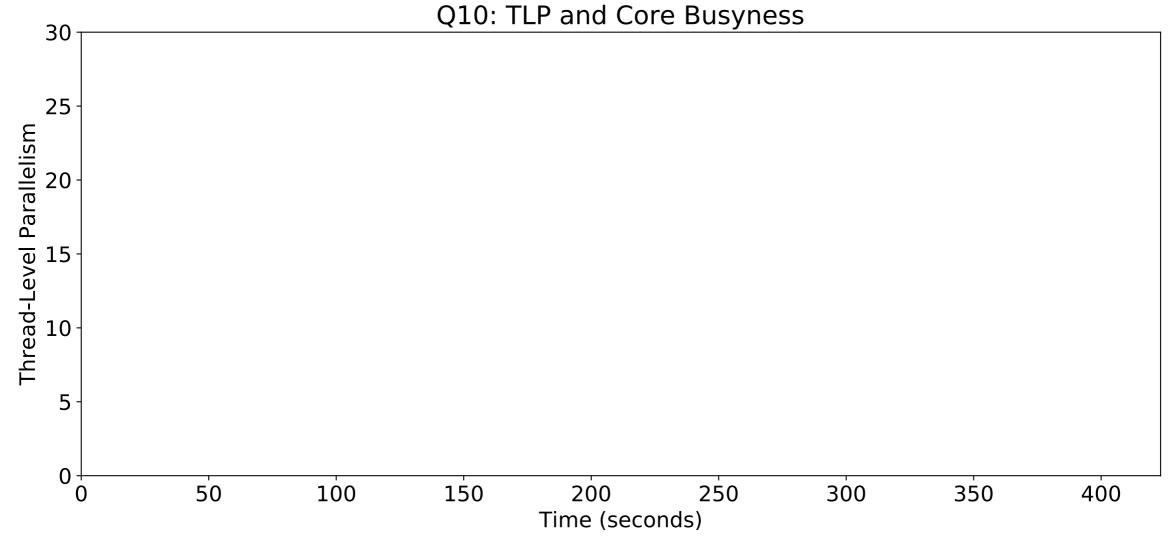




Proactively restrict the number of active cores to just meet the workload.

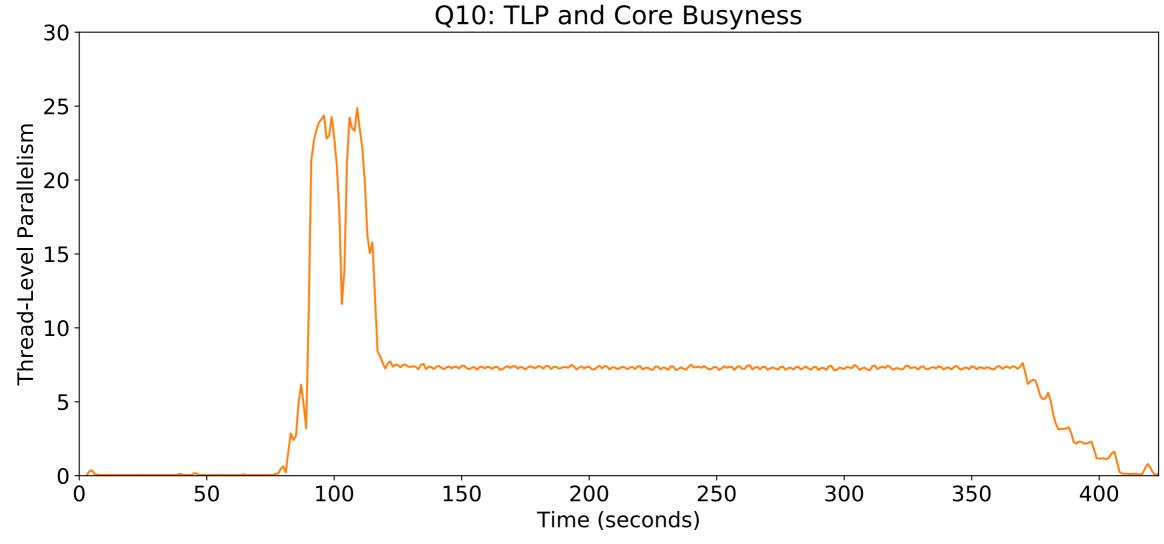


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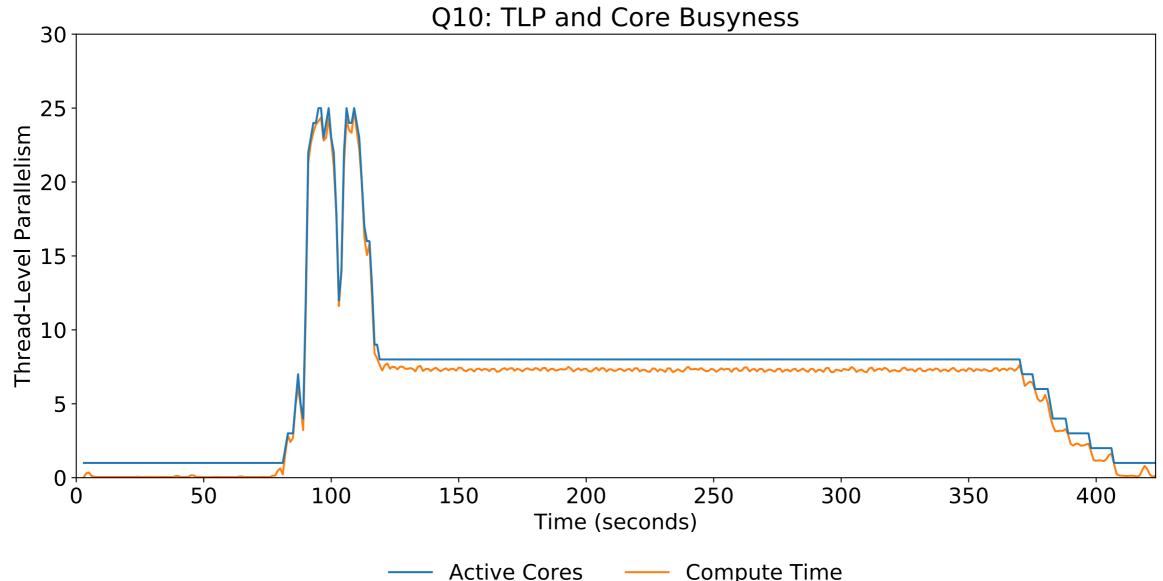


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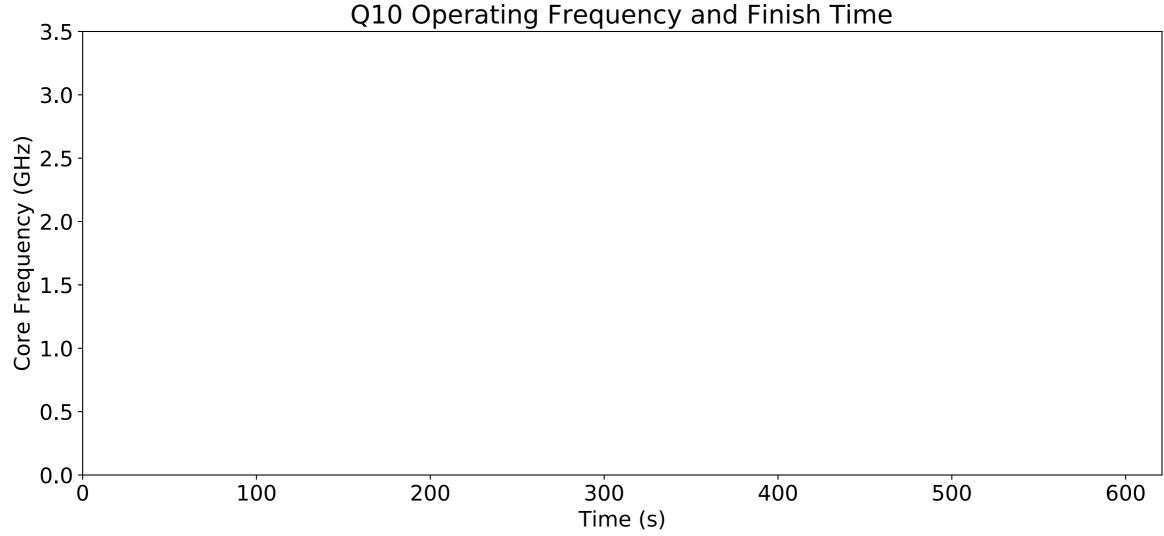
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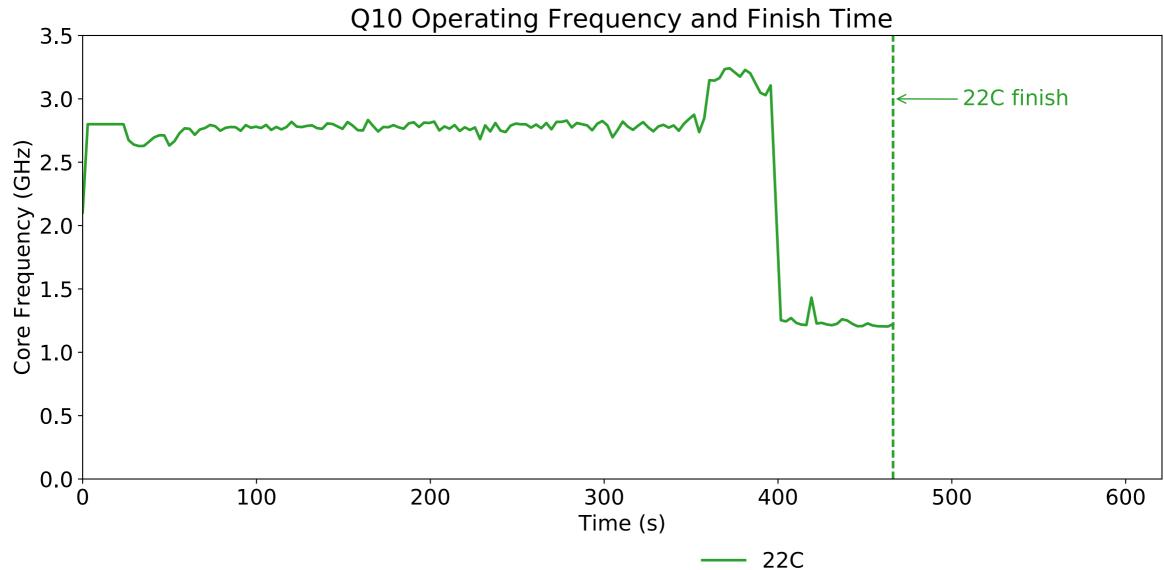




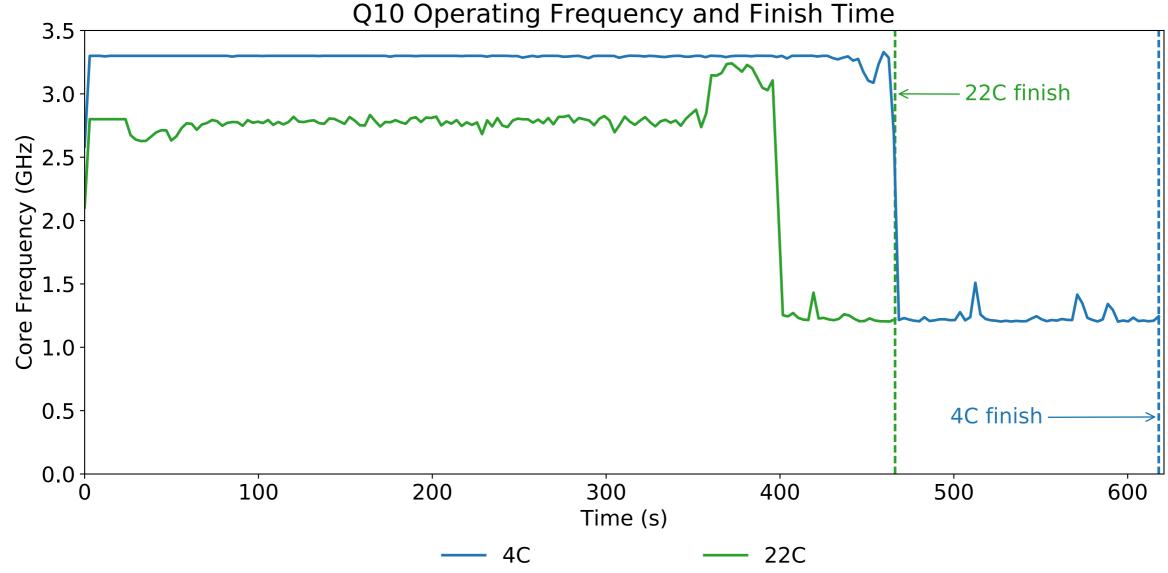




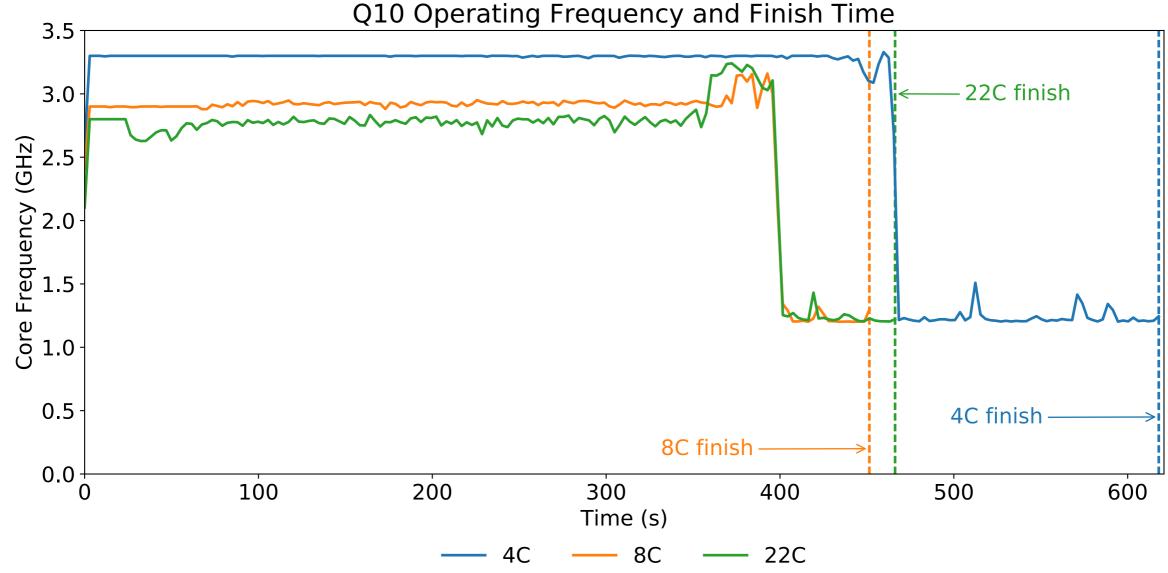






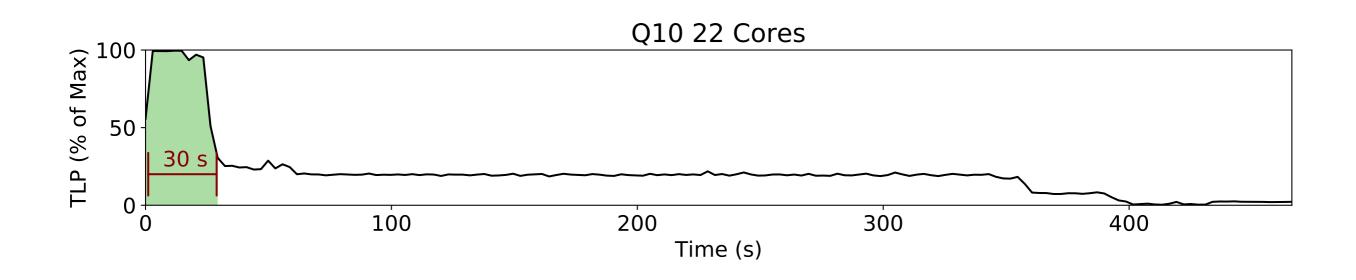




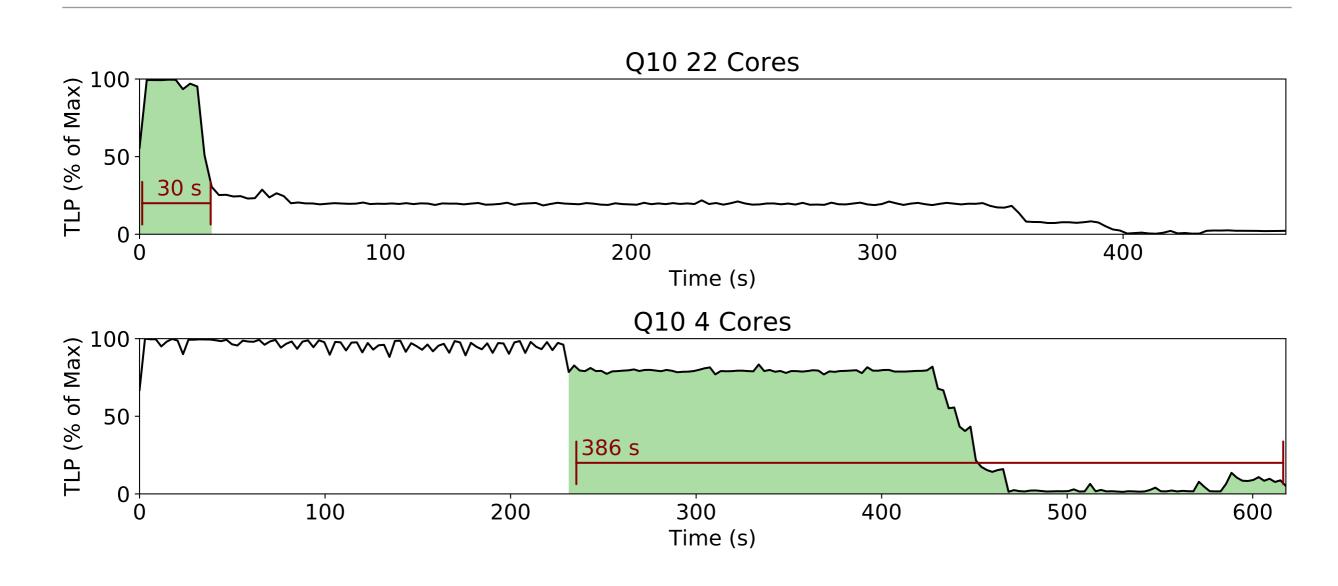




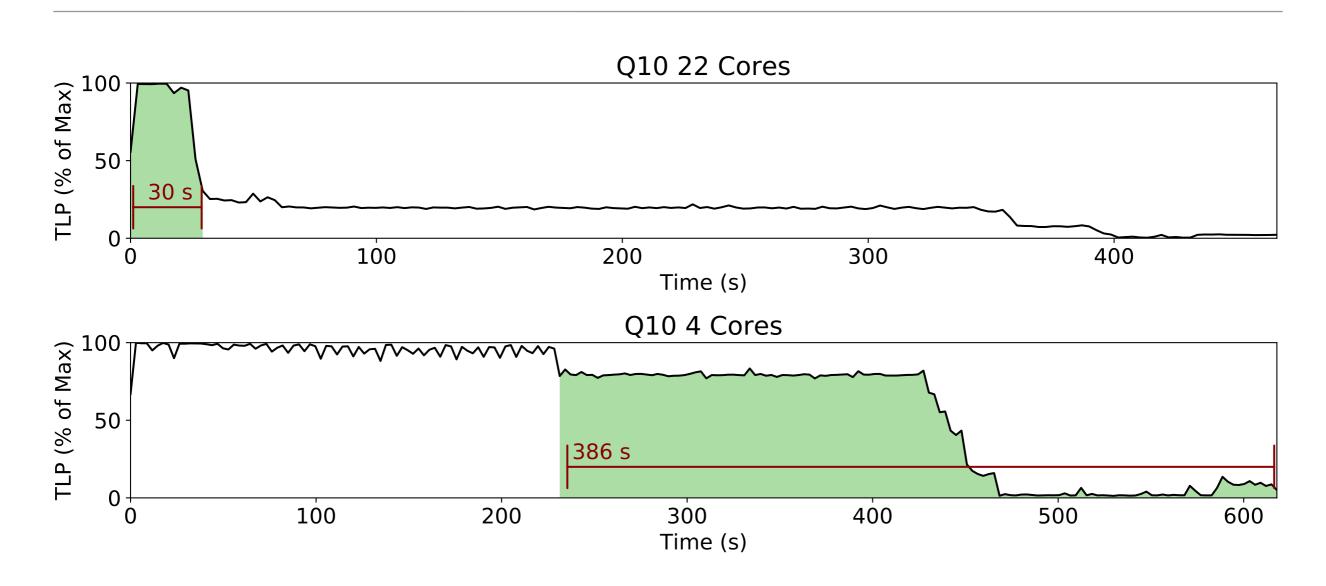








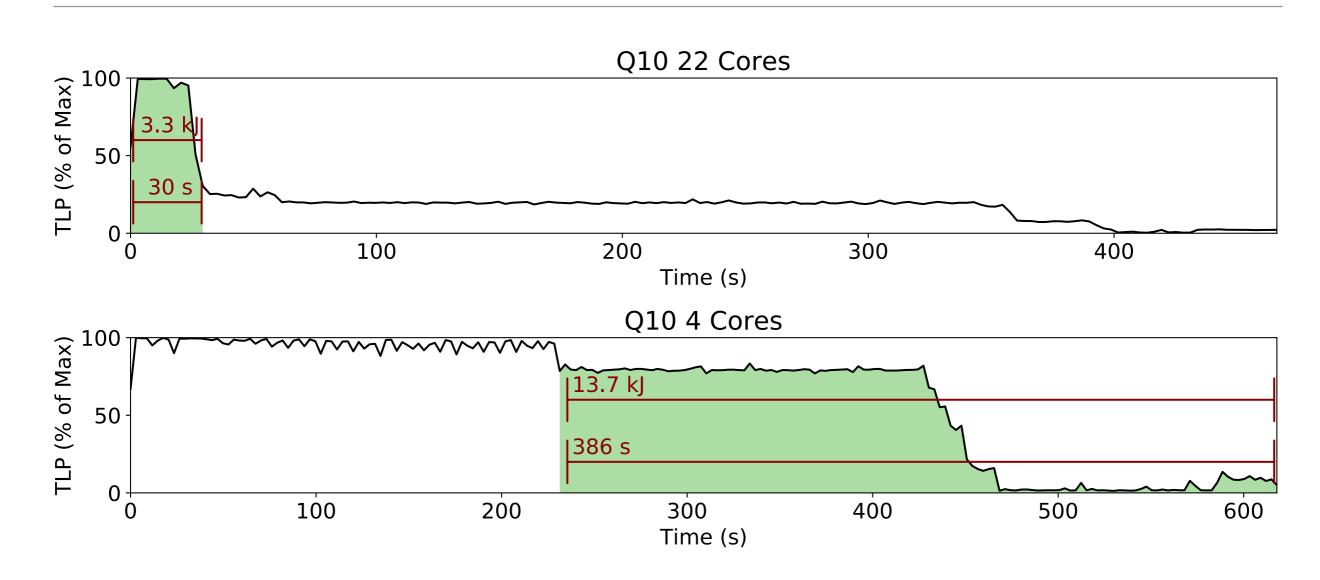




Query 10 could finish in 416 seconds: a 13.5% speedup.



Core Packing—Better Approximation



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Furthermore, energy consumption decreases by 30%.

Analysis



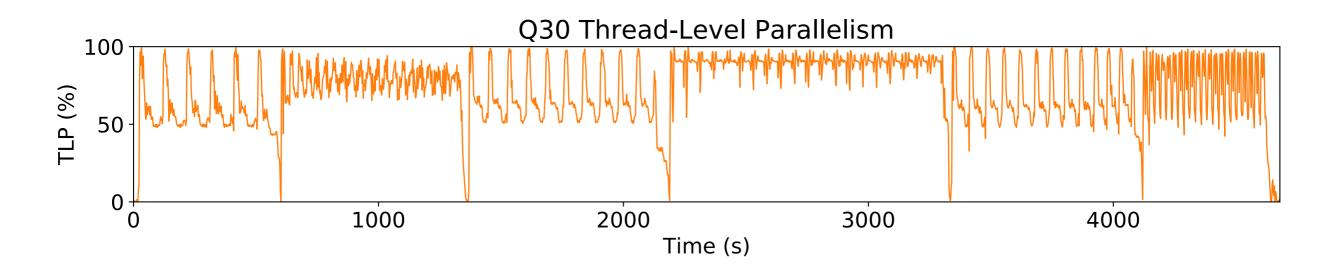
Analysis

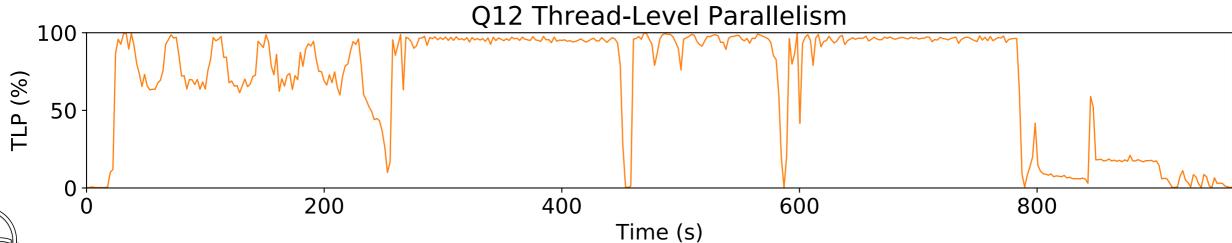
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 $(freq_{Max} - freq_0)$ Turbo Boost ceiling room





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 $\frac{freq_{TB} - freq_0}{freq_0}$ Fractional increase in frequency

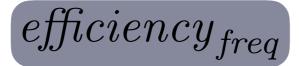


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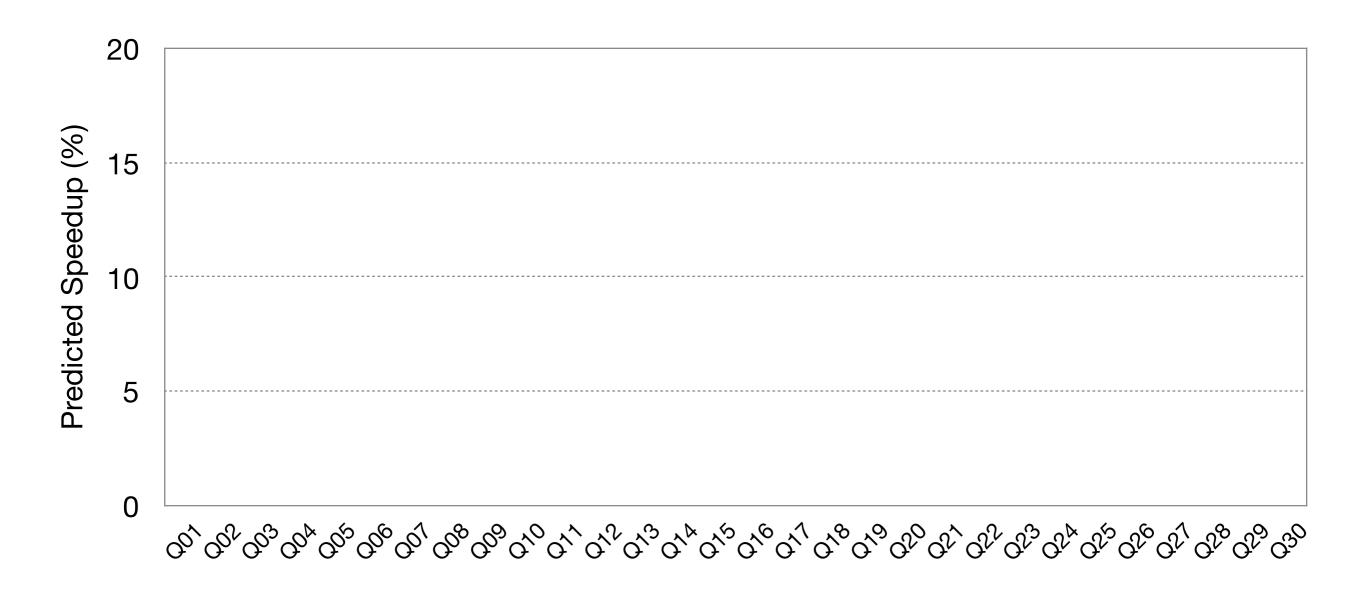
Fractional increase in frequency



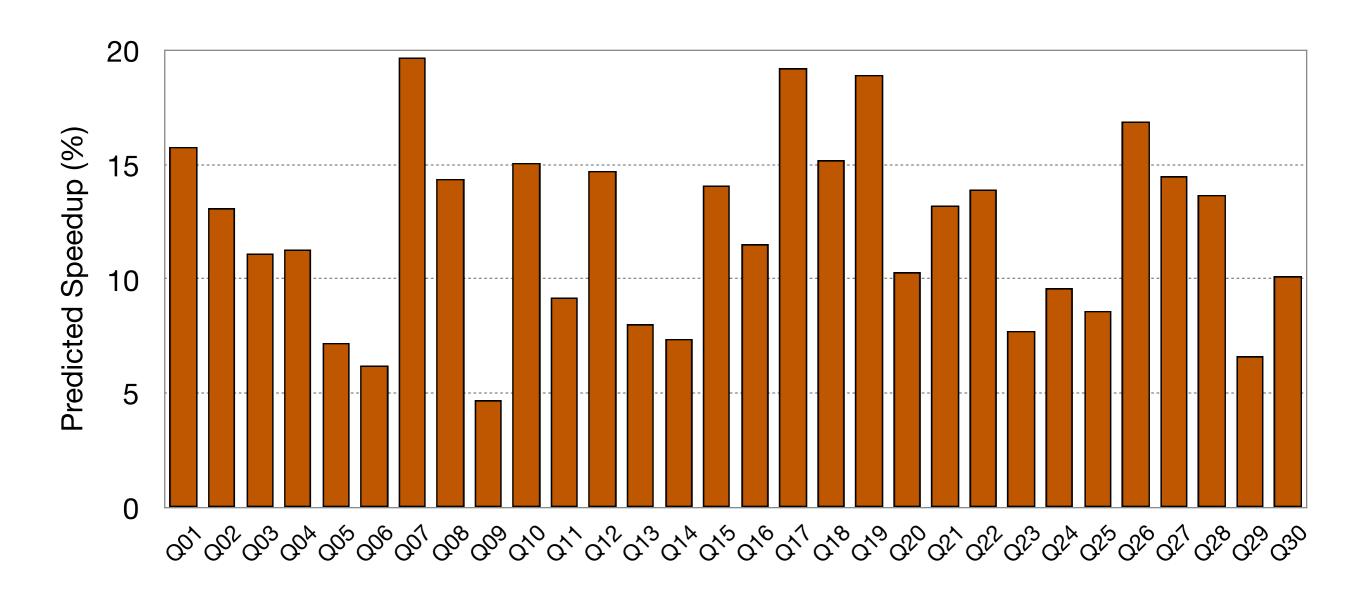
Efficiency of frequency scaling



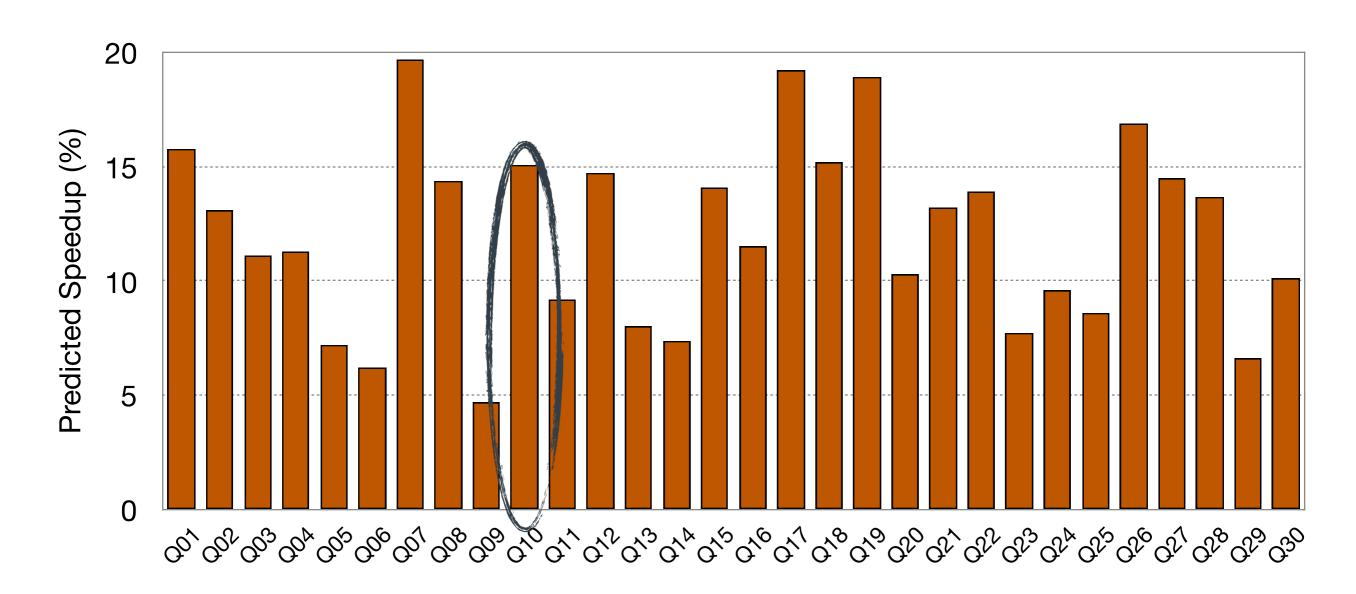












Notably, Q10's modeled speedup of 15.1% is remarkably close to our predicted speedup of 13.5%.



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Current hardware and software cooperatively undermine Turbo Boost's ability to accelerate execution.

We propose core packing to aid Turbo Boost and predict 4-20% speedup.



Amdahl's Law is Alive and Well In Big Data Analytics

Questions

http://www.tpc.org/tpcx-bb/default.asp

